A High Speed Full Adder Circuit using 3 Transistor XOR Gates for Arithmetic Operations of VLSI System

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Abstract— The necessities to obtain better speed, this paper list to a change in parameter of full adder circuit that has been proposed by using 3T XOR gate combining CMOS with pass transistor logic. The design that has been given shows a significant improvement in propagation delay constrain. The proposed adder gives better propagation delay in comparison with the previously existing reference design. The 50nm technology has been used to investigate the performance of 8T full adder circuit and the complete design is simulated with the help of LTSPICE.

Key words: CMOS, Enhancing Speed, Full Adder, MGDI, Transistor Count Minimization and XOR gate

I. INTRODUCTION

Most of VLSI applications utilize full adder as a basic building block in arithmetic operations, like as digital signal processing, embedded system, image and video processing and microprocessor. In order to obtain a better response, we basically work on three different areas such as minimizing the number of transistors, enhancing the speed and reduce the power loss. Furthermore areas including the minimum number of transistors, enhancing speed, reducing power loss, high throughput, full voltage-swing, chip area, driving capability and layout regularity focused recently [1]-[8]. In most of the devices that are commonly used in daily life, such as calculator cellular phone, mobile, computer and laptop require high speed along with low power consumption [3]. These requirements lead to the further researches in the designing of full adder circuit.

The design has been implemented with the help of a full adder circuit [7] along with an XOR gate consisting of 3 transistors [3] as per literature. Other sections that have been used in this paper are previous work related to the design, 3 transistor XOR gate and 8T full adder design, simulation results along with the final conclusion.

II. PREVIOUS WORK

A full adder is a combinational circuit. It performs the arithmetic sum of three 1-bit inputs: A, B and a carry in, C, which gives SUM, S, and carry-out, CARRY as 1-bit results.

$$SUM = (A \text{ XOR } B) \text{ XOR } C \quad (1)$$

$$CARRY = A.B + C.(A \text{ XOR } B) \quad (2)$$

The circuit shown above figure 1 has been used as a base circuit in the paper. In this circuit eight transistor full adder is designed by using MGDI technique. As per the equation (1) by cascading of two input XOR gates of MGDI cells the output is obtained. Similarly, according to equation (2) two transistors multiplexer of MGDI cell has been used to obtain carry output. There are four terminals in MGDI cell that are D (common diffusion node of both transistors) G (common gate input of NMOS and PMOS transistors), N (the outer diffusion node of MOS transistor) and P (the outer diffusion node of PMOS transistor) [7]. In figure2 shown below, an OR logic gate has been modeled with the help of MGDI cell. The source to NMOS is given through the input 'A' and the drain of PMOS is connected to 'B' input. The gate terminal G of PMOS and NMOS both is connected to input 'A'.

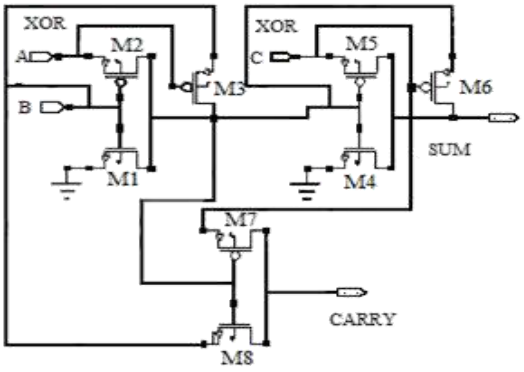

Fig. 1: 8T Full Adder using MGDI technique

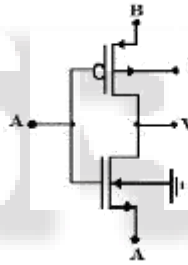

Fig. 2: MGDI OR logic gate

The working of MGDI cell can be easily described with the help of the table 1 shown below. The input voltage, output voltage, threshold voltage for PMOS, threshold voltage for NMOS and supply voltage are denoted by respectively Vin, Vout, Vtp, Vtn and VDD.

INPUTS		OPERATING REGIONS	
A	B	PMOS	NMOS
0	0	Linear	Cut-off
0	1	Cut-off	Linear
1	0	Linear	Cut-off
1	1	Linear	Linear

Table 1: The Working Region Corresponding To the Inputs of the MGDI Cell

When the PMOS works in the linear region, output voltage is found to be between (Vin-Vtp) and VDD and similarly the NMOS works in the linear region, output voltage is found to be between 0 and (Vin-Vtn). The condition for being in the cutoff region of PMOS is Vin > VDD + Vtp and similarly the condition for NMOS is Vin < Vtn.

The output voltage is supposed to be equal to the Vin, but because of the threshold drop the output voltage is reduced. The degradation (Vin-Vtn or Vin-Vtp) in the voltage can be reduced by increasing the width of the channel while keeping the channel length constant. [3]

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Through the literature [9], we can easily deduce the formula (equation 3) that shows the relation between threshold voltage of the transistor design and its width and length.

$$V_T = V_{T0} + \gamma(\sqrt{V_{SB} + \phi_0} + \sqrt{\phi_0}) - \alpha_l \frac{t_{OX}}{L}(V_{SB} + \phi_0) - \alpha_V \frac{t_{OX}}{L} V_{DS} - \frac{t_{OX}}{W}(V_{SB} + \phi_0) \quad (3)$$

Where V_{T0} represents zero bias threshold voltage, γ represents bulk threshold coefficient, ϕ_0 is $2\phi_F$, where ϕ_F denotes the Fermi potential, t_{ox} is the thickness of the oxide layer and α_l, α_V and α_W are process dependent parameters.

On the basis of equation (3) shown above, we can regulate the threshold voltage by controlling width W and lent L of the channel. The design 8T full adder figures out the voltage degradation problems. On the basis of literature [5] when voltage degradation takes place, it has been found the speed of the cell decreases and also signal integrity degrades.

III. Proposed 8T Full Adder

The proposed full adder is consisting of the 3T XOR and a carry out module. In the literature [1]-[8] different model of the XOR gate has been given.

A. 3T XOR Gate

The model of XOR gate has been taken from the literature [3]. The design (figure 3) posses 3 transistors, which is based upon a latest version of CMOS inverter and a PMOS pass transistor. The design operates as a CMOS inverter when the input B is high. Through the input A and output voltage is the complement to each other. CMOS inverter gives high impedance when input B is at the low logic. When the input B is low, then pass transistor M3 turns ON and the output obtained as similar to input A. For A=1 and B=0, the voltage degradation would take place across the transistor M3 and the output would be less than Vin. The reduction in output voltage can be reduced with increasing the width to length ratio of transistor M3. One another problem arises due to the flow of current from transistor M3 to transistor M1 when A=1 and B=0. This problem can be minimized by reducing the width to length ratio of transistor M1 [3]. The proposed design of XOR gate has a width to length ratios for M1, M2 and M3 transistors are 8/1, 30/1 and 100/1 respectively as shown in fig.3 for 50nm technology (according to the supply voltage 1V).

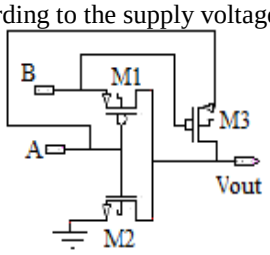

Fig. 3: Design of 3T XOR gate

B. Proposed 8T Full Adder

The 8T full adder is proposed in the paper uses 3T XOR gates along with 2T multiplexer. The relationship for SUM and CARRY has been expressed below-

SUM= A XOR B XOR C

CARRY= AB + BC + AC

LTSPICE with 50nm technology has been used for simulating proposed full with 1V supply voltage. For reducing threshold voltage the width of transistors increased, must be decreased. With the help of figure 4 we can easily look up the aspect ratio (width to length ratio) of each transistor.

IV. Simulation and Performance Analysis

The analysis of the performance 8T full adder has been done by using LTSPICE using 50nm technology. The supply voltage through simulation is about 1 volt. There are total eight transitions through the three inputs which establish each and every possible testing environment for the proposed 8T full adder. The respective waveforms that are generated for all transitions with the help of inputs to the full adder A, B and C are shown in the figure 4 shown below. In order to measure delay of the full adder we take the time difference between inputs and outputs when both reaches the same voltage level 50% while the transition from high to low or low to high. The possible transitions are 000, 001, 010, 011, 100, 101, 110, 111. All the transitions have been passed through the simulated model and the delay for every transition has been calculated. By taking average for each transition the delay for the full adder is measured [7]. The simulation waveforms of full adder through which the transitions have been examined as shown below (figure 5).

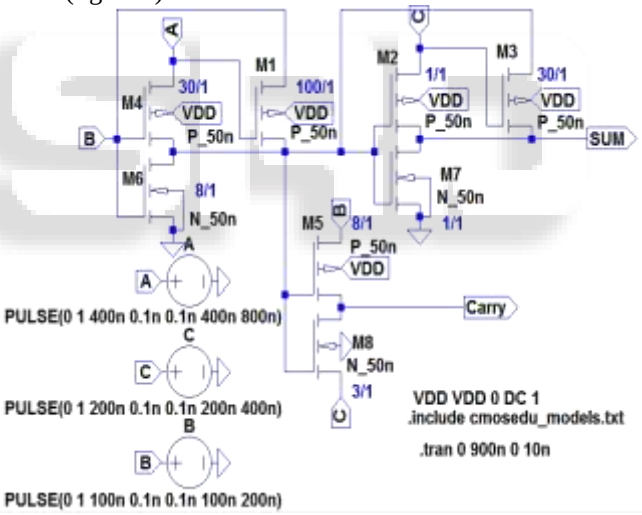

Fig. 4: Design of the eight transistor full adder

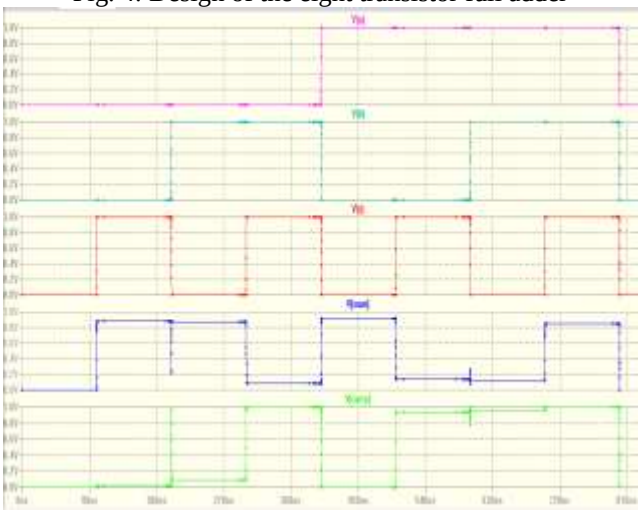

Fig. 5: Simulated Waveform of proposed full adder

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	Reference Full Adder	Proposed Full Adder
Propagation Delay (ps)	16.05	4.2186

Table 2: A Simple Comparison between the Full Adder Circuits

V. CONCLUSIONS

The conclusion can be easily deducted through the table 2. The propagation delay has been reduced from 16.05 ps to 4.2186 ps. The result is found to be given 3.8 times better propagation delay than the previously proposed adder. 50nm technology has been used to design and analyze the 8T full adder. The comparison between the reference full adder and proposed full adder has been shown in the table 2. Thus we can see that the proposed full adder gives a huge reduction in propagation delay with lesser transistors and low supply voltage.

REFERENCES

[1] M. Vesterbacka, "A 14-transistor CMOS full adder with voltage swing nodes," in Proc. IEEE Worksh. Signal Process. Syst., pp. 713-722, Oct. 20-22, 1999.
[2] D. Radhakrishnan, "Low-voltage low-power CMOS full adder," in Proc. IEE Circuits Devices Syst., vol. 148, pp. 19-24, Feb. 2001.
[3] S.R. Chowdhury, A. Banerjee, A. Roy, H. Saha, " A high speed 8 transistor full adder design using novel 3 transistor XOR gates," International Journal of Electronics, Circuits and Systems 2, 217(2008).
[4] Subodh Wairya, Garima Singh,Vishant, R. K.Nagaria, S. Tiwari, "Design Analysis of XOR (4T) based Low Voltage CMOS Full Adder Circuit," International Conference On Current Trends In Technology, „Nuicone – 2011" 08-10 December, 2011.
[5] M. Zhang, J. Gu, and C.-H. Chang, "A novel hybrid pass logic with static CMOS output drive full-adder cell," in Proc. of the 2003 International Symposium on Circuits and Systems (ISCAS '03), vol.5, pp. 317 - 320, 25-28 May 2003.
[6] Chiou-Kou Tung; Yu-Cherng Hung; Shao-Hui Shieh; Guo-Shing Huang, "A Low-Power High-Speed Hybrid CMOS Full Adder for Embedded Systems" IEEE Design and Diagnostics of Electronic Circuits and Systems, pp.1- 4, Apr., 2007.
[7] A. Morgenshtein, A. Fish, I. A. Wanger, "Gate-Diffusion Input (GDI): A power efficient method for digital combinational circuits," IEEE Trans. on Very Large Scale Integration (VLSI), vol. 10, No. 5, pp. 566-581, 2002.
[8] R.Uma, P. Dhavachelvan, "Modified Gate Diffusion Input Technique: A New Technique for Enhancing Performance in Full Adder Circuits," 2nd International Conference on Communication, Computing & Security [ICCCS-2012], vol.6,page 74-81, 2012.
[9] Y. Tsividis, Mixed Analog-Digital VLSI Devices and Technology, Singapore: McGraw Hill, 1st edition, 1996.

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