Design of High Speed All Digital Phase Lock Loop for FM Application
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Abstract—All Digital Phase Lock Loop (ADPLL) is contributing in advancement in digital communication and control system since 1980. In this paper “High speed ADPLL for FM application” is proposed. The ADPLL is designed using phase detector, digital loop filter and increment-decrement counter. Here the speed of ADPLL is increased by using novel multiplexer based increment-decrement counter. The ADPLL using these blocks are simulated by using Xilinx 14.5. It is observed that the delay of proposed ADPLL is less compare to existing ADPLL [1]. Further, the proposed ADPLL is used to generate FM modulation by using interpolator method.

Key words: PLL, ADPLL, FM Modulation

I. INTRODUCTION
The phase lock loop (PLL)[2] is a feedback control system. The primary functionality of a PLL is to compare the phase and frequency of the input signal with that of feedback signal, then adjust the feedback signal till the phase error becomes completely zero. For communication systems and many modern electronics and electrical system, the PLL act as an important part. In the communication field, PLL is used to generate and modulate the signal. The modulation and demodulation of signal is mainly used in the receiver system hence it is implied that PLL is inevitable for the receivers. The PLL has much more applications like frequency synthesis, clock recovery and clock generation in communications and networking system.

The analog PLL has many disadvantages like, it occupies more implementation area, more delay, and also it is easily susceptible to noise due to analog component in the design. So there is a necessity of PLL, to be designed in digital, so that it is used in digital communication system. In order to overcome the disadvantages of the analog PLL, digital phase lock loop are proposed. Due to the digital design, it has minimum area, minimum delay and low power consumption.

Most of the researchers have conducted research on the PLL[3,4] to realize higher speed minimum chip area and minimum phase noise PLLs are classified into four types they are

The enhanced phase locked loop[5] was designed by using the combination of a 4-state PFD (phase and frequency detector) with a latching circuit. In this method lock time is reduced by using initial bias circuit. After the PLL, the early effort on the digital PLL was concentrated on replacing analog component partially with digital component. The author Westlake [6] was the first person worked in this direction in year of 1960. He was used a sample and hold circuit to take the advantage of digital voltage controlled oscillator

The ADPLL design based on the double edge triggered D flip flop [7] was designed. This type of ADPLL resolves the key issues like by-direction zero crossing and phase detection. The whole design is coded by using HDL and implemented on FPGA. The synthesis report shows that the speed of whole loop is increased by twice compared to conventional PLL. Due to the use of DETDFF(double edge triggered D flip flop) there is reduction of 33% power dissipation.

The survey of many papers, illustrated. some limitation in PLL like delay, area and power. In this paper a high speed ADPLL for FM application is designed. Here the speed is increased by using a novel multiplexer based increment-decrement counter.

The paper is divided in the several sections as follows: Section II provides the ADPLL design and describes all the building blocks of the ADPLL. Section III describes the simulation result of ADPLL design. Section IV provides the Conclusion and future scope of the paper.

II. PROPOSED METHODOLOGY
A. Design of ADPLL
The ADPLL resembles the conventional PLL in structure but all the components and intermediate signals are digital in nature. The figure1 shows the basic block diagram of ADPLL.

Fig 1: Block diagram of ADPLL

The basic operation of an ADPLL [9] mainly depends on three important building blocks they are namely a digital phase detector, digital loop filter, and digital increment and decrement counter as a controlled oscillator. The brief discussion of each of these blocks are given in the subsequent sections.

1) Phase Detector
The main building block of ADPLL is a phase detector. here the phase detector is considered as a simple XOR gate. Based on the inputs of the phase detector the error signal is produced at the output side of phase detector. The inputs to the phase detector are input reference clock signal and the output of the divide by B counter. The output of phase detector is given as input to digital loop filter
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**2) Digital Loop Filter**

The digital loop filter consist of top up counter and bottom up counter. Both of these counter counts in upward direction and they are independent on each other. whenever the DOWN/UP_BAR=1 then bottom up counter is activated and it starts counting in the upward direction when half of the maximum count reaches it produces borrow signal. Since at half of the maximum count the MSB will be produced. The top up counter is enabled when DOWN/UP_BAR=0 and it start counting in upward direction when half of the maximum count reaches it produces carry signal. Carry or the borrow signal given to the input of increment – decrement counter

![Block diagram of digital loop filter](Fig. 3: Block diagram of Digital loop filter)

A counter has a modulus control which decides the maximum count value.

![Flowchart of digital loop filter](Fig. 4: Flowchart of digital loop filter)

**3) Increment-Decrement Counter (ID counter)**

In the design of the increment-decrement counter a novel multiplexer based addition and deletion of clk pulse is designed instead of using toggle flip flop, so that delay can be reduced. In this paper depending on the condition of the carry and borrow pulse the frequency is adjusted. If the carry and borrow pules are zero then it performs divided by two operation. This divided by 2 is achieved by using clock divider circuit. If carry is logic one and borrow is logic zero then adding the one clock pulse to clock signal. If carry is low and barrow high then one clock pulse is deleted from the clock signal. If both carry and barrow are high this is invalid condition. The clock signal applied to ID counter is two times the center frequency. The output of the ID counter is given as input to divided by B counter. The figure5 shows the novel increment-decrement counter based on multiplexer

![Block diagram of increment and decrement counter](Fig. 5: Block diagram of increment and decrement counter)

The table 1 gives the information about when to add clock pulse, delete clock pulse and divide the clock signal depending on the carry and borrow condition.

<table>
<thead>
<tr>
<th>Carry (c)</th>
<th>Barrow (b)</th>
<th>Operations</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>Divide clk by 2</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>Add clk pulse</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>Delete clk pulse</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>Invalid condition</td>
</tr>
</tbody>
</table>

**Table1: Table of increment and decrement counter**

![Flowchart of increment and decrement counter](Fig. 6: Flowchart of increment and decrement counter)

**4) Divided by B counter**

Since 2Bfo clock is applied to the input of the increment-decrement counter to satisfy the sampling theorem so that aliasing effect can be avoided. Here B is variable which is multiplied to center frequency to avoid the aliasing. So the output of increment-decrement counter should be divided by B. The output of the divided by B counter is feed back to the input of phase detector

**5) Frequency modulation using designed ADPLL**

The designed ADPLL is used in the frequency modulation technique since the designed ADPLL has high speed. The output period width ADPLL will decrease and increase, these decrease and increase period width will be responsible for different modulation frequency.

![Basic block diagram of FM](Fig. 7: Basic block diagram of FM)
As shown in the basic block diagram, the frequency modulation scheme consists of ADPLL, interpolator, accumulator, and numerically controlled oscillator. The ADPLL is used to generate different message signals, which are given as input to the interpolator. The interpolator is used to get the required signal level for the modulation of frequency. Here, the interpolation factor is taken as a factor of 32 between two successive signal samples. The interpolator calculates the difference and divides it by 32. The division is done by shifting the new FM data by one bit before the subtraction and four bits after the subtraction. Afterwards, the output is added to the previous FM input data on each clock.

The interpolation operation is performed by using one adder for the addition operation, some registers for storage, and a subtractor for the subtraction of the signal. The block diagram shows the detail explanation of the interpolator.

The interpolator output is given to the input of the accumulator. The accumulator function is to add the message signal and the carrier signal and store the result. The output of the accumulator is given as input to the numerically controlled oscillator, which produces the output that is frequency modulated wave depending on the input signal to the numerically controlled oscillator.

The NCO built in block used to generate the sinusoidal signal with independent frequency. It generates a discrete value representation of a waveform. The NCO contains a look-up table that contains a finite set of values that are used to generate sinusoidal waves. Depending on the input signal value, the NCO generates different frequencies by using the look-up table. The frequency modulation scheme is used in the communication field, particularly in the FM receiver.

### III. RESULTS AND DISCUSSION

This paper intends to implement ADPLL and as an application of ADPLL, FM is considered. The performance of ADPLL is evaluated based on the performance parameter shown in Table 2. The parameters considered for evaluation are mainly speed, lock range so that it is suitable for FM application, capture range, and jitter uncertainties. As per the design parameters and central frequency, we get a lock range of 90kHz, capture range of 24kHz, and jitter uncertainties of 200ns. As discussed, designed values of parameters are central frequency is 200kHz.

The value of $A=3$ is the modulus control value of the digital loop filter. $B$ is variable which is multiplied to the center frequency = 8.

In this section, the result evaluation is done to evaluate performance by simulating functionality using Xilinx platform. Functional simulation is done to verify the performance.

#### A. Simulation results of ADPLL for lock range

The fig 9 shows the simulation results of lock range of ADPLL. The lock range is defined as the range of frequencies over which PLL will track the input frequency signal and remains locked. For the 200kHz central frequency as per design specification, the lock range observed is 11μs. Here, inputs to the ADPLL are input clock and the feedback clock signal.

![Fig 9: Simulation result of lock range](image)

LOCK RANGE: $1,003,000\text{ ns} - 992,000\text{ns} = 11,000\text{ns} = 90\text{kHz}$

#### B. Simulation result of ADPLL for Jitter calculation

It is locking uncertainty expected between output and input.

![Fig 10: Simulation result of Jitter calculation](image)

Jitter uncertainty: $992,500\text{ ns} - 992,300\text{ns} = 200\text{ns}$

#### C. Simulation result of Capture range

The frequency range the PLL is able to lock in starting from the unlocked condition. The fig 10 shows the simulation result of capture range of ADPLL.

![Fig 11: Simulation result of capture range](image)

Capture Range: $23,125\text{ ns} - 14,687\text{ns} = 8,438\text{ns}$

<table>
<thead>
<tr>
<th>Parameters</th>
<th>ADPLL design</th>
</tr>
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</table>
A (loop modulus control) | 8  
B (variable) | 8  
\(f_0\) (center frequency) | 200kHz  
Lock range | 11000ns  
Capture range | 8438 ns  
Jitter uncertainty | 200ns

Table 2: Design parameters of ADPLL

IV. COMPARISON OF THE RESULT

Table 3: Delay Comparison of the existing ADPLL and proposed ADPLL

<table>
<thead>
<tr>
<th></th>
<th>Delay</th>
</tr>
</thead>
<tbody>
<tr>
<td>Exiting ADPLL</td>
<td>12.99ns</td>
</tr>
<tr>
<td>Proposed ADPLL</td>
<td>5.504ns</td>
</tr>
</tbody>
</table>

A. FM modulation result

The input to the FM is output of the ADPLL. Since the output period width of ADPLL will decrease and increase, these decrease and increase period width will be responsible for different modulation frequency as shown in the figure 12.

Fig. 12: Simulation result of FM modulation

The fig 13 shows the frequency spectrum of FM modulated wave from the wave form we got frequency range 200MHz to 230MHz.

Fig. 13: Frequency spectrum of FM modulated wave

V. CONCLUSION AND FUTURE SCOPE

In this paper high speed ADPLL for FM application is designed. Here speed of ADPLL is increased by using novel multiplexer based addition and deletion clock pulse in the increment – decrement counter instead of using toggle flip flop which was used in the previous ADPLL. Further the designed ADPLL output is used to generate FM modulated wave using interpolation method. The designed ADPLL has a lock range of 90kHz, Capture range of 24kHz and Jitter uncertainty 200ns. The designed ADPLL has delay 5.504ns and it gives frequency modulation in the range of 200MHz to 230MHz.

In future, the proposed design can be extended to more range of frequency by designing variable counter in the loop filter. The resolution N bit can be increased to obtain more lock range of frequency, and also in FM modulator interpolator method is replaced with any other alternate method which can improve the range of frequency modulation.

REFERENCES


