Design and Implementation of Power and Area Optimized 16-Bit 5T SRAM Array using Cadence 90nm Technology

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Abstract— As the technology scaling goes on increasing, reduction in power consumption and over all power management on chip are main challenges for any size below 100nm due to increased complexity and area reduction. Semiconductor memories are most important subsystem of modern digital systems. Many advance processors now have on chip instructions and data memory using SRAMs. Thus, improving the power efficiency of a SRAM cell is critical to the overall system power consumption. This project is based on the design of a CMOS Five-transistor SRAM cell (5T SRAM cell) for very high density and low power applications. This paper investigates the effectiveness of 5T SRAM circuit design technique along with power consumption and chip density analysis. Simulation and analytical results show that proposed cell has correct operation during read/write mode. The new cell size is 21.66% smaller than a conventional 6T SRAM cell using same design rules with no performance degradation. The new 5T SRAM cell contains 68.84% less power consumption with respect to the 6T SRAM cell and also the average power consumption of 16 bit 5T SRAM array has been reduced by 69.17% when compared to 16-bit 6T SRAM Array using cadence 90nm technology.

Key words: SRAM, CMOS, Cadence

I. INTRODUCTION

Memory is the foremost part of computer and microprocessor situated systems. It's used to preserve the information or data in terms of binary number (zero or one). The data that are used for programs and the application code are also stored in the memory. Memory is being used for both temporary and permanent storage of data in any digital system. In general recollections are of two forms: "Random Access Memory" (RAM) and "Read Only Memory" (ROM). Since ROM is designed once and is used just for reading, it is also referred as permanent memory whereas RAM is used for both read and write operation. RAM is again classified in two types: SRAM and DRAM. In this work power minimized SRAM memory system is designed.
Power dissipation is the main constraint once it involves portability. The mobile device client demands additional options and extended battery life at a lower value. About 70% of users demand longer speak and stand-by using time as important cell cell-phone feature. Prime 3G demand for operators is power potency. Customers wish smaller & sleeker mobile devices. These need high levels of element integration in advanced processes. However advanced processes have inherently higher Leakage current. Therefore there's a need to bother more on reducing Leakage current to cut back power consumption.

This work aims to present power minimized SRAM even at retaining good efficiency and good data retention. At the same time due to the fact the inducement of this project, the primary objectives are listed as following:

- To increase the performance of a processor by employing power and area optimized SRAM array
- To minimize the power consumption of a memory system
- To lessen the number of transistors and hence area of entire systems

The rest of the paper is organized as follows. Section 2 discusses the fundamentals of SRAM. Section 3 presents the methodology for developing a power and Area optimized 5T SRAM. Section 4 includes the Design and Implementation details of 16 bit 5T SRAM array system. Section 5 gives the Results and Analysis and Section 6 concludes the paper.

II. FUNDAMENTALS OF SRAM

An SRAM (Static Random Access Memory) is designed in order to fulfil two needs. One is to facilitate a direct interface between the system memory and the CPU at a very high speed which cannot be achieved by the DRAMs and other one is to employ SRAMs instead of DRAMs in systems that require very low power consumption.

In the first role, the SRAM is used as a cache memory providing interfacing between DRAMs and the CPU. In its second role SRAM technology is gaining lot of demands because of its low power applications. As the refresh current of DRAM is multiple times greater than that of the SRAM standby current, SRAMs are widely used in most of the portable devices. Fig. 1 shows a typical PC microprocessor memory configuration.

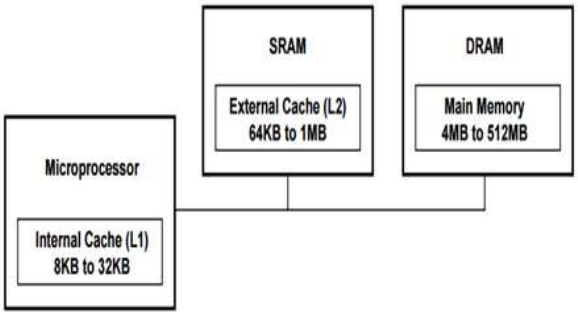

Fig. 1: Typical PC Microprocessor Memory Configurations

A. Basics of SRAM Array Architecture

Generally Memory systems are designed using memory cells for storing the data and a number of peripheral circuits for accessing these memory cells. The general SRAM architecture is shown in Fig. 2.

The General memory architecture is made up of array of memory cells which are surrounded by the support circuitry to decode the addresses and perform the data read and write operations. The memory is organized in terms of rows and columns of memory cells which are generally known as word lines and bit lines respectively. The SRAM array consists of 2n rows * 2m columns. A row is selected

by inserting one of the 2n word lines which is the output of an n-bit address decoder. A Column is selected by inserting one of the 2m bit lines in order to perform read as well as write operation.

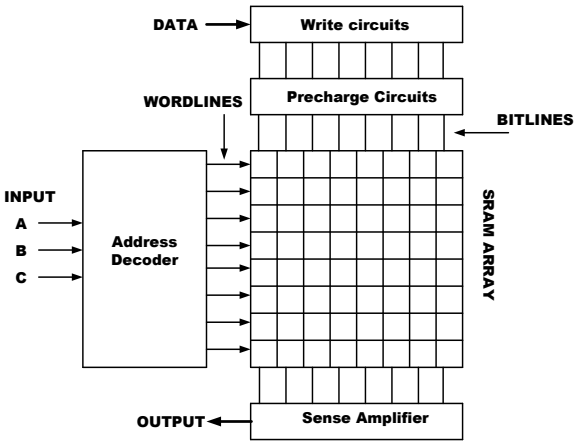

Fig. 2: General SRAM Memory Architecture

During the read operation, Precharged circuits will charge the bit line to a high value close to the supply voltage and the sense amplifier on each column is employed to read the data. In write operation, the write circuit will force the bit line or its complement of selected column to '0'or '1' and the input data will be written onto the internal nodes of the selected cell.

B. Device Working

The SRAM cell consists of two cross coupled inverters which are connected to the other circuits by means of two access transistors as shown in Fig. 3. When the SRAM cell is not addressed both the access transistors are in OFF state thereby keeping the data stable by being latched within the flip-flop. Since SRAM is a volatile memory it requires continuous power supply to retain the data otherwise the stored data is lost. But data does not leak away as in case of DRAM, because of which the SRAM does not require repeated refresh cycle to hold the data.

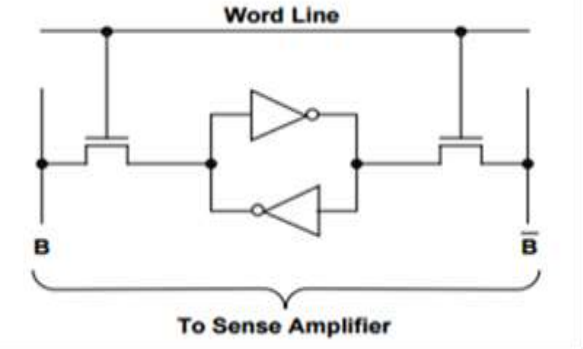

Fig. 3: SRAM Cell

III. METHODOLOGY

With an intension to achieve higher memory density and very low power consumption a new 5T SRAM cell has been designed and employed in 4 words x 4 bits SRAM array. This 5T SRAM cell consists of one transistor less than that of the 6T SRAM cell, this is how the memory density is increased with reduced power consumption. The circuit diagram of 5T SRAM cell is as shown in Fig.4. It is designed for 90nm technology node with a power supply of 1.1V. The working of this cell is as follows:

- In idle state, that is when none of the operations are performed on the cell, feedback cutting transistor (M5) is turned ON and 'N' node is pulled up to VDD through this transistor.
- During write operation, if data to be stored id logic '1'then M2 and M3 are turned ON and there exists a positive feedback between ST node and STB node. Therefore ST node is pulled up to VDD whereas STB node is pulled down to VSS. If the data to be stored is logic '0' then only M4 is turned ON and as 'N' node is maintained at VDD through M5, the STB node is pulled up to VDD.

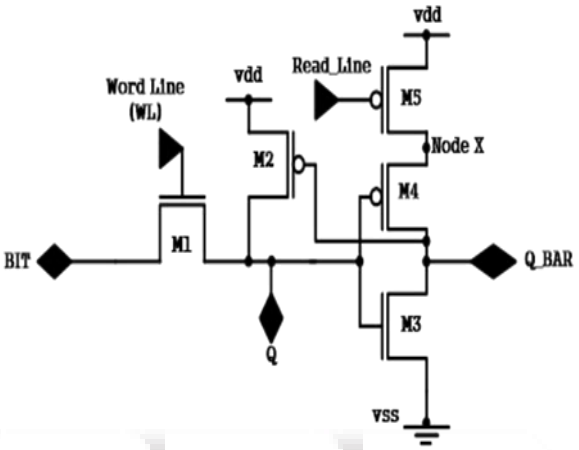

Fig. 4: CMOS Five-transistor SRAM cell

A. Write and Read Operations

When write operation is to be performed read line signal has to be maintained at VSS so that the feedback cutting transistor M5 is turned ON and node ' N' is pulled up to VDD. While performing write operation, memory cell will go through the following steps.

1) First the data to be written is loaded onto the bit line
2) Word line is asserted (WL=1)
3) Now the data loaded onto the bit line is passed through the access transistor M1 to the rest of the circuit. This step includes two cases:

a) Data to be written is '0': In this case, the access transistor M1 and the load transistor M4 are ON. Therefore the ST node is pulled down to GND through M1 and STB node is pulled up to VDD through M4

b) Data to be written is '1': In this case, the access transistor M1, drive transistor M2 and load transistor M3 are ON. Therefore ST node is pulled up to VDD through M1 and STB node is pulled down to VSS through M3. Now M2 will be turned ON creating positive feedback between M2 and M3.

4) After writing the data, memory cell will enter into the idle state in which the word line and bit line are asserted to Vidle and VSS respectively.

While performing the read operation, memory cell follows steps as listed below:

1) The read line signal is made high (RL=1).
2) Bit lines are discharged to GND (BL=BL'=0).
3) Word line is asserted to VDD (WL=1). Here two cases are considered:

a) When ST node is at logic '1', bit line voltage is pulled up to high voltage through NMOS access transistor. This bit line voltage is referred as VBL-HIGH.
b) When ST node is at logic '0', the voltage of both ST node and the bit line are equalized.
4) Word line is deactivated and read line is returned to GND
5) Now the sense amplifier is turned ON in order to read the data on the bit line.
6) After the completion of read operation, again the cell will enter into the idle mode.

IV. DESIGN AND IMPLEMENTATION

This complete project is carried out using Cadence virtuoso tool. With the aid of circuit diagram of each module we have constructed the schematic view of each basic block using cadence virtuoso schematic editor. For each and every schematic a symbol is created and later constructed a test circuit in order to verify its functionality. By providing the test patterns in accordance with the truth table output waveforms are generated thereby verifying their functionality. The circuit simulation is performed using cadence virtuoso ADE spectre.

A. Decoder

In this project Lyon-Schediwy decoder is used for address generation. This decoder has an advantage of smaller area and faster access time as it uses lesser number of transistors than AND/NAND decoder which is used for address generation. The schematic view is drawn using cadence virtuoso schematic editor as shown in Fig. 5. The functionality of this circuit is verified using cadence virtuoso ADE spectre.

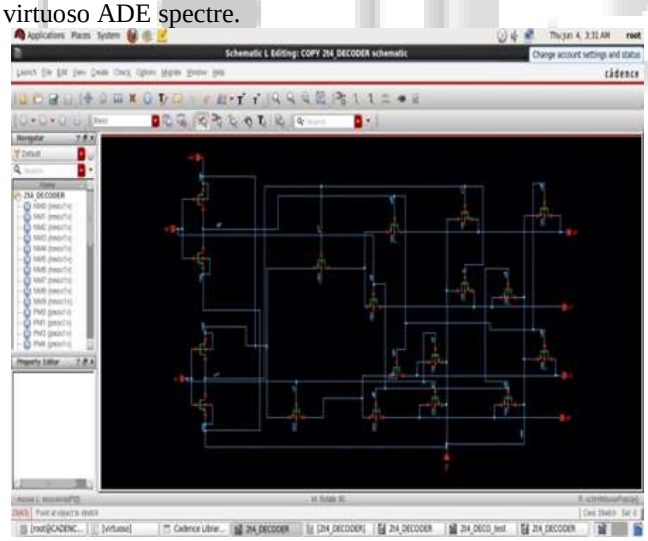

Fig. 5: Schematic of Lyon-Schediwy 2:4 Decoder

B. Sense Amplifier

A sense amplifier is a part of the read circuitry which plays an important role when information is to be read from the memory. Its function is to sense the low voltage levels from a bit line that represents a data bit (1 or 0) which has been saved in a memory cell, and then amplify the small voltage swing in order to make it as recognizable data bit. So that data are often taken properly by logic outside the memory. The schematic view of sense amplifier is as shown in Fig. 6.

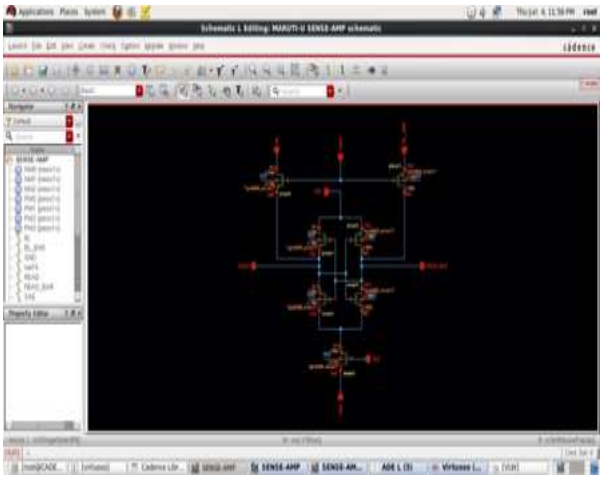

Fig. 6: Schematic of Sense Amplifier

C. Write Circuit

The function of write circuitry is to write the required data into the memory cell. For this operation to be performed, bit line has to be loaded by the data to be written along with the assertion of write enable signal. In this project, most widely used schematic view of write circuitry is constructed as shown in Fig.7.

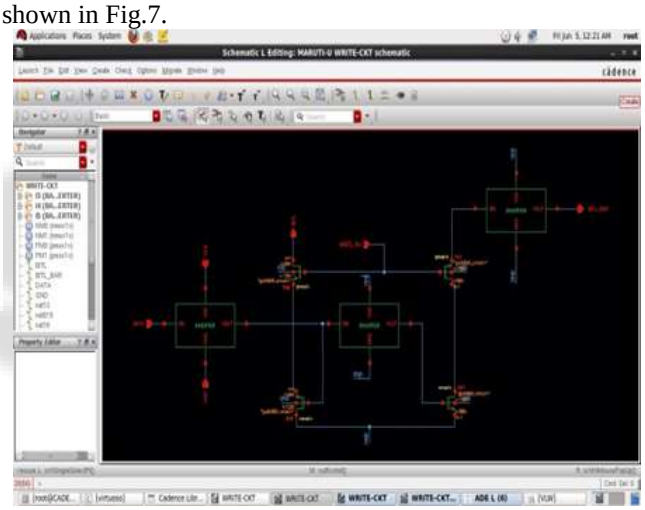

Fig. 7: Schematic of Write Circuit

D. Precharge Circuit

The Precharge circuit is segregated from BL and BL' throughout read and write operation. One Precharge circuit is connected to each column to Precharge the BL and BL' to logic 1 when memory is in idle state. The schematic view and simulation waveforms of Precharge circuit are as shown in Fig.8.

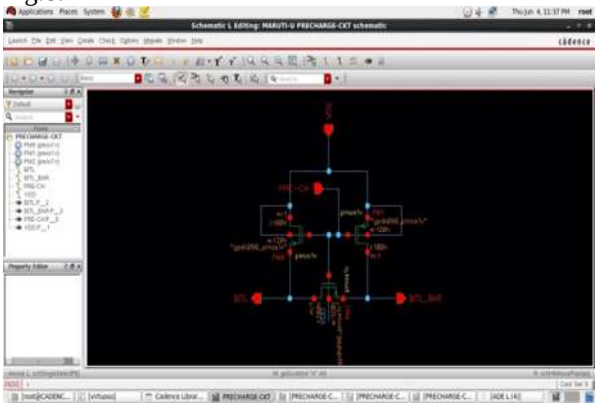

Fig. 8: Schematic of Precharge Circuit

E. Proposed 5T SRAM Cell

This cell is an improved form of the 8T and 6T SRAM memory cells. As previously explained 6T SRAM suffers from excessive amount of leakage power and 8T SRAM cell, which is a modified form of 6T SRAM cell suffers from reduced memory density though it achieves less leakage power. So in order to overcome these drawbacks of 6T and 8T SRAM cells 5T SRAM cell is designed which achieves less leakage power along with high memory density. The schematic as well as simulation waveforms of 5T SRAM cell are as shown in Fig. 9 and Fig. 10 respectively.

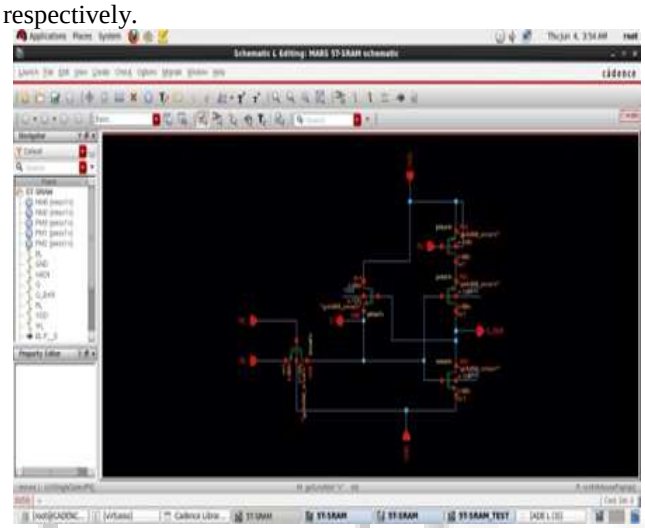

Fig. 9: Schematic of proposed 5T SRAM cell

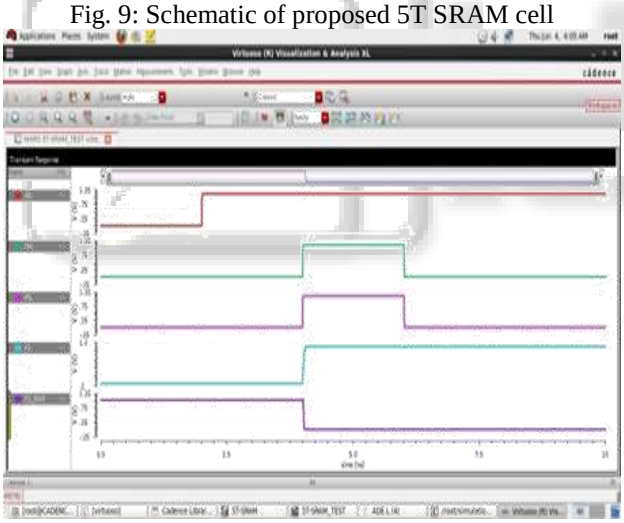

Fig. 10: Simulation waveform proposed of 5T SRAM cell

F. Sixteen Bit Memory Array Using 5T SRAM Cell

The 4words x 4bits memory array system is designed using sixteen 5T SRAM cells. These are arranged in the form of 4 rows and 4 columns, each of which are of 4 bits. In this project a 2:4 Lyon-Schediwy decoder is employed in order to address each of the 4 words in all the four rows. The schematic view of 4words X 4bits memory system that includes all sixteen 5T SRAM cells, one 2:4 decoder, four sense amplifiers, four write drivers and four Precharge circuits is shown in Fig. 11.

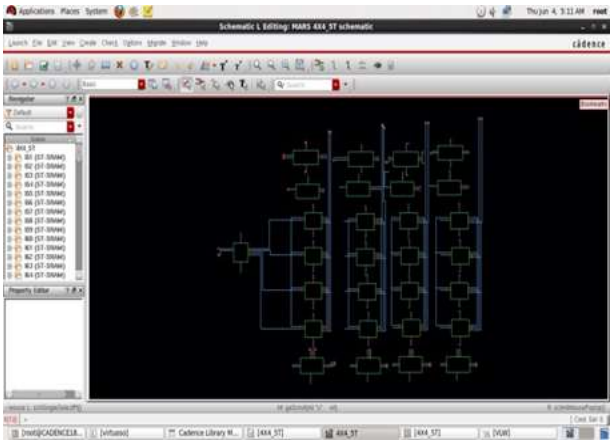

Fig. 11: Schematic of 16 bit Memory Array using 5T SRAM Cell

The functionality of this memory system is checked by providing it with specific input patterns and then analyzing the generated output waveforms, which is as shown in Fig. 12.

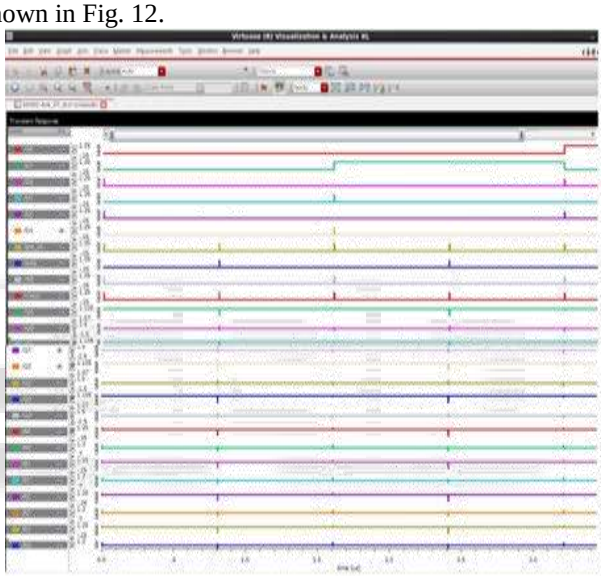

Fig. 12: Simulation waveform 16 bit Memory System using 5T SRAM cell

In this project first the layout of 5T SRAM cell is constructed as shown in Fig. 13 and the layout of final 4 words x 4 bits 5T SRAM memory array is as shown in Fig. 14. Further we have carried out the physical verification of this layout by means of DRC(Design rule check), LVS check (Layout versus schematic) and RC (parasitic) extraction.

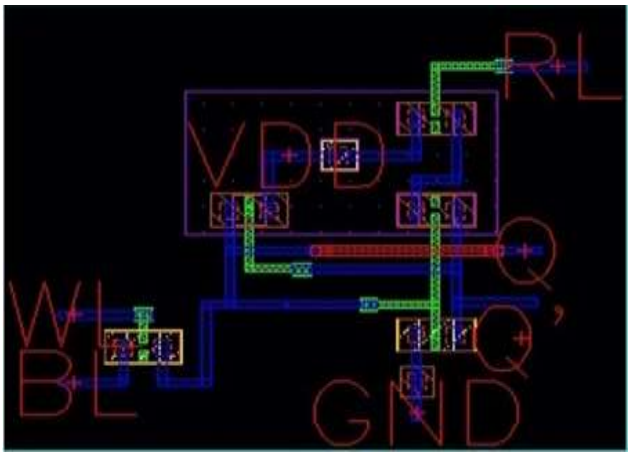

Fig. 13: Layout of 1 bit 5T SRAM Cell

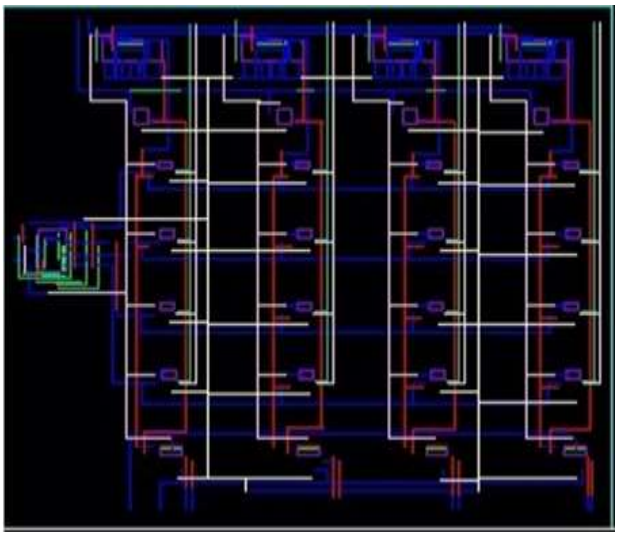

Fig. 14: Layout of 16 bit 5T SRAM Array

V. RESULTS AND ANALYSIS

In this project the power consumption of 8T, 6T and proposed 5T SRAM cells have been measured and are as listed in Table. 1. Along with this, power consumption of 16 bit SRAM array using 8T, 6T and proposed 5T SRAM cells are also measured and these values are as listed in Table. 2.

1 Bit SRAM cell	Average power consumption in Watts
8T	28.58m
6T	5.917µ
5T	1.844µ

Table 1: Average Power Comparison for 1 Bit SRAM Cell

16 Bit SRAM array	Average power consumption in Watts
8T	457.8m
6T	957.2µ
5T	295.1µ

Table 2: Average Power Comparison for 16 Bit SRAM Array

By observing the average power consumption values from the above tables it can be noticed that the average power consumption of 1 bit 5T SRAM cell is reduced by 68.84% when compared to 1 bit 6T SRAM cell and also the average power consumption of 16 bit 5T SRAM array has been reduced by 69.17% when compared to 16-bit 6T SRAM Array.

VI. CONCLUSION

In this project initially 6T SRAM cell, 8T SRAM cell and 5T SRAM cells are designed and verified for their functionality. The power consumption of these cells is also measured with the help of Cadence Virtuoso ADE Visualization and Analysis XL Browser and XL Calculator. Here it is observed that power consumption of 5T SRAM cell is very much less than the 6T and 8T SRAM cells. In the next part a 16 bit SRAM array is designed using 8T SRAM cell, 6T SRAM cell and proposed 5T SRAM cell and later verified for their functionality along with power measurement of these memories. By these power measurement values it is noticed that the average power consumption of 1-bit 5T SRAM cell has been reduced by 68.84% when compared to 1-bit 6T SRAM cell and it is also reduced by 69.17% when16-bit 5T SRAM array is compared with 16-bit 6T SRAM array. The feasibility of this design for the product fabrication is also verified by designing the layout and checking it through physical verification tools such as DRC, LVS and RCX.

REFERENCES

[1] V.De and S. Borkar, "Technology and Design Challenges for Low Power and High Performance," in Proc. Int. Symp. Low Power Electronics and Design, 1999, pp. 163-168.
[2] M.D.Powell, S.H.Yang, B.Falsafi etal.. Gated – VDD:A circuit technique to reduce leakage in cache memories. In proceedings of International Symposium on Low Power Electronics and Design, July 2000
[3] Timothy Kam, Shishpal Rawat, Desmond Kirkpatrick, Rabindra Roy, Gregory S. Spirakis, Naveed Sherwani, and Craig Peterson. EDA challenges facing future microprocessor design. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 19(12), December 2000.
[4] S.Borkar, T. Karnik, S. Narendra, J.Tschanz, A. Keshavarzi, and V. De, "Parameter variations and impact on circuits and microarchitecture," 2003. 775920 338-342.
[5] K. Khare, N. Khare, V.K. Kulhade and P. Deshpande, "VLSI Design And Analysis Of Low Power 6T SRAM Cell Using Cadence Tool," IEEE International Conference on Semiconductor Electronics, Nov. 2008, pp. 117–121.
[6] N. Rahman and B.P. Singh, "Design of Low Power SRAM Memory Using 8T SRAM Cell", International Journal of Recent Engineering and Technology, March 2013, pp. 123–127.
[7] MichaelWieckowski, Martin Margala.University of Rochester,NY, United states.
[8] Takeda K. et al., A read-static-noise-margin-free SRAM cell for low-VDD and high-speed applications, IEEE Journal of Solid-State Circuits, vol. 41, no. 1, pp. 113{121, 2006.
[9] S.M. Kang, Y. Leblebici, CMOS Digital Integrated Circuits-Analysis and Design, 3rd ed., WCB McGraw-Hill, 2003, pp. 220-222.
[10] S. Akashe, S. Bhushan and S. Sharma, "High Density and Low Leakage Current Based 5T SRAM Cell Using 45 nm Technology," International Conference on Nanoscience, Engineering and Technology (ICONSET), Nov. 2011. pp. 346– 350.
[11] J. M.Rabaey, A.Chandrakasan and B. Nikolic, Digital Integrated Circuits, 2nd ed.,Prentice-Hall of India Private limited, 2005, pp. 272-282.
[12] S.Babu,Solid State Device and Technology, 3rd ed., Pearson Publication, 2008

