Analysis and Modification of D Flip Flop using Different Techniques

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Abstract— Low power design has become one of the primary focuses in both analogue and digital VLSI circuits. The pertinent choice of flip flop topologies is an essential importance in the design of VLSI integrated circuits for high speed and high performance speed of circuits. This paper enumerates low, high speed design of D flip flop .It presents various techniques to minimize the power consumption of CMOS circuits. In this D flip flop is implemented using Static CMOS, CCMOS, GDI, GDI MUX, POWER PC,TG and TSPC Techniques. The simulation is done on TANNER EDA Tool at 180nm &130nm Technologies.

Key words: Low Power, Propagation Delay, CMOS, GDI, GDI MUX, TG, POWER PC, C2MOS & TSPC, D Flip flop

I. INTRODUCTION

From the day when transistor was invented in 1947, low area, low power and high speed are the primary issue for researchers. In the modern technology ,low power consumption have emerged a key design constraint over the last few years due to increasing demand of portable systems in the vlsi circuit design.so latches and flip flops have a direct impact on power consumption and speed of the VLSI system. Flip flops are the important timing elements in the digital circuit. Flip flop is a bistable circuit which stores a logic state if 0 and 1.The d flip flop is the most useful storage element in the digital circuit design. In the design of sequential circuits a major challenge is to design an efficient D flip flop. In this paper several different architectures of D flip flops have been implemented and simulated using TANNER EDA TOOL at 180nm &130nm technologies. The comparison is also done on the basis of Transistor count, Delay, power.

II. POWER DISSIPATION IN CMOS CIRCUITS

CMOS technology provides better results than TTL (Transistor Transistor logic).but due to increasing demand of portable systems the two parameters affect the performance of CMOS design. These parameters are as Follows.

- Power dissipation
- Delay in CMOS circuits

The total power consumption in CMOS circuits is given by

$$P_{total} = P_d + P_{sc} + P_s$$

Where P_d is the Dynamic power dissipation. P_{sc} is the short circuit power dissipation .P_s is the static power dissipation.

- Dynamic power dissipation is due to charging and discharging of load capacitances during switching.
- Short circuit power dissipation is occur when short circuit current flows during the brief transient when the pull up and pull down tran sistor conduct at the same time.
- Static power dissipation is due to leakage current drawn by reversed biased diodes between n-well and substrate.

III. IMPLEMENTATION OF D FLIP FLOP USING DIFFERENT DESIGN TECHNIQUES

A. Static CMOS D Flip Flop

Static CMOS uses N-MOS pull down and P-MOS pull up transistors together in a complementary way. It has good noise margin, high speed and easier to design. D flip flop based on Conventional static CMOS logic style has low power consumption than TTL. The circuit of Static CMOS DFF is shown in Figure.1.This circuit operates at 1.5 v in 130nm & 1.8v in 180 nm technologies. The clock frequency is 100MHz.The circuit is implemented using TANNER EDA Tool.

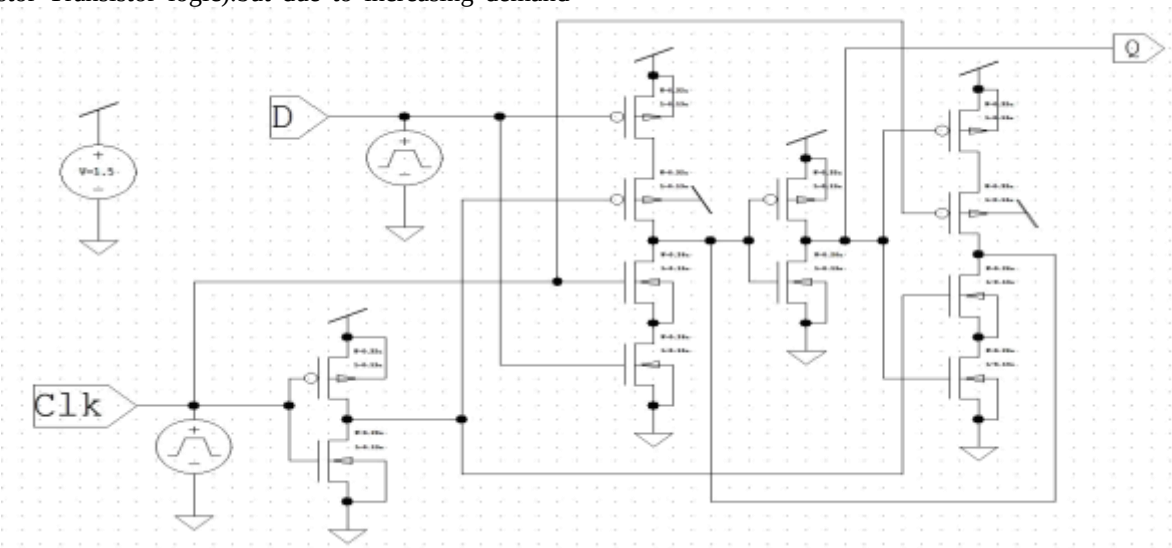

Fig. 1: Static CMOS DFF

The otput waveform of Static CMOS is shown in figure 2

Fig. 2: Output waveform of Static CMOS DFF

B. C^2MOS D FLIP FLOP

Clocked CMOS is composed of a static logic circuit with tri state output network (made up of FET M1&M2).that is controlled by ϕ and ϕ .

- When, both M1 and M2 are active, and become to a standard static logic gate
- When $\phi = 1$, both M1 and M2 are cutoff, so the output is in HI-Z state.

The circuit OF Clocked CMOS D flip flop is shown in Figure.3.And the output waveform of Clocked CMOS D flip flop is shown in figure.4.

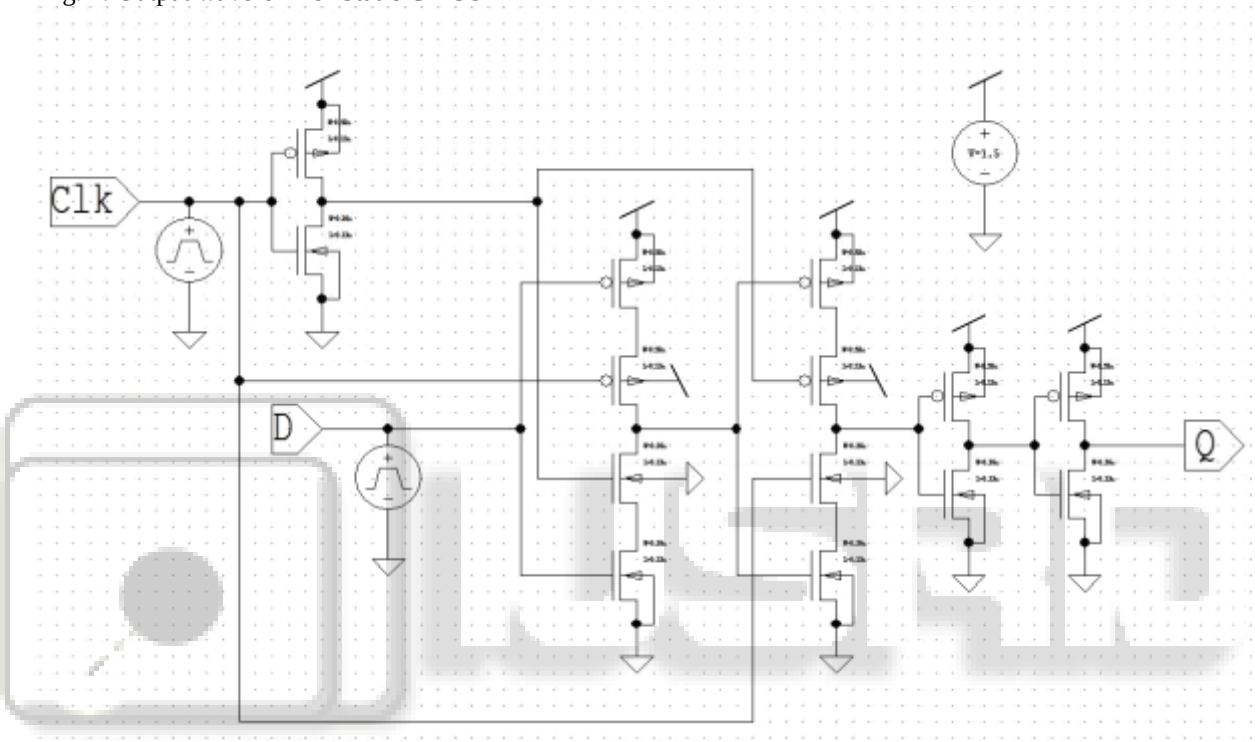

Fig. 3: Clocked CMOS DFF

The output waveform of this is shown below in figure 4.

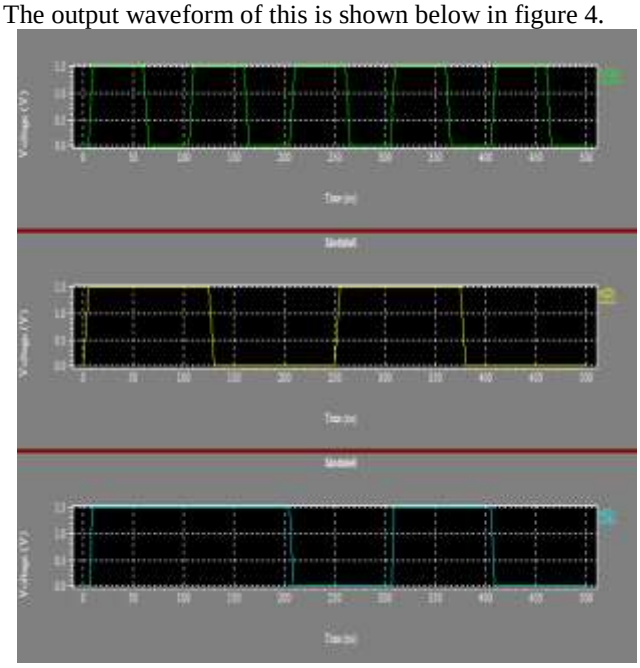

Fig. 4: Output waveform of Clocked CMOS DFF

C. GDI D FLIP FLOP

GDI(Gate Diffusion Input) allow implementation of wide range of complex logic functions using only two transistors. This method is used to design low power circuits with reduced number of transistors.A basic GDI cell contain four terminals G(Common Gate input for both NMOS and PMOS transistors).P(Outer diffusion node of PMOS),N(Outer diffusion node of NMOS) and D(common diffusion node of both transistors).A basic GDI Cell is shown in figure.5.

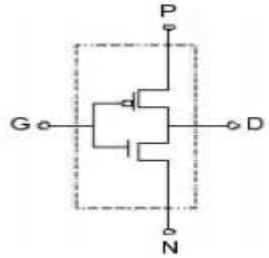

Fig. 5: Basic GDI Cell

The circuit of GDI D flip flop is shown in figure .6 and output waveform is shown in figure.7

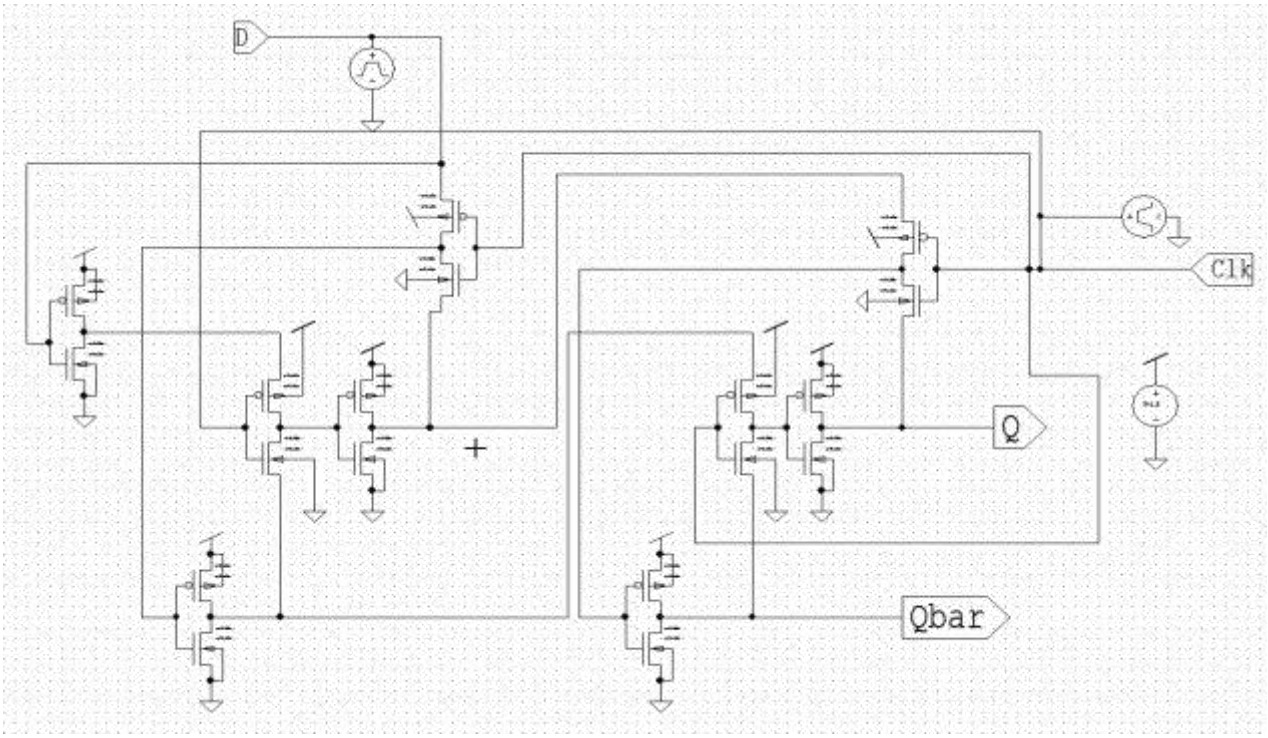

Fig. 6: GDI DFF

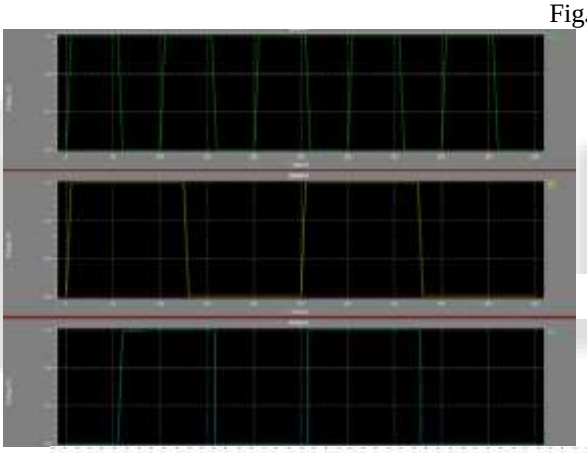

Fig. 7: Output waveform of GDI DFF

D. GDI MUX D FLIP FLOP

GDI Multiplexers are composed of single pair of transistors and a cross coupled pair of inverters. First multiplexer is connected to the system clock and its inputs are connected to the D input and feedback loop. The inverted signal is the input to the second latch, with the feedback loop connected to the opposite input of the multiplexer. The circuit of GDI MUX D flip flop is shown in figure.8 and the output waveform of GDI MUX DFF is shown in figure 9.

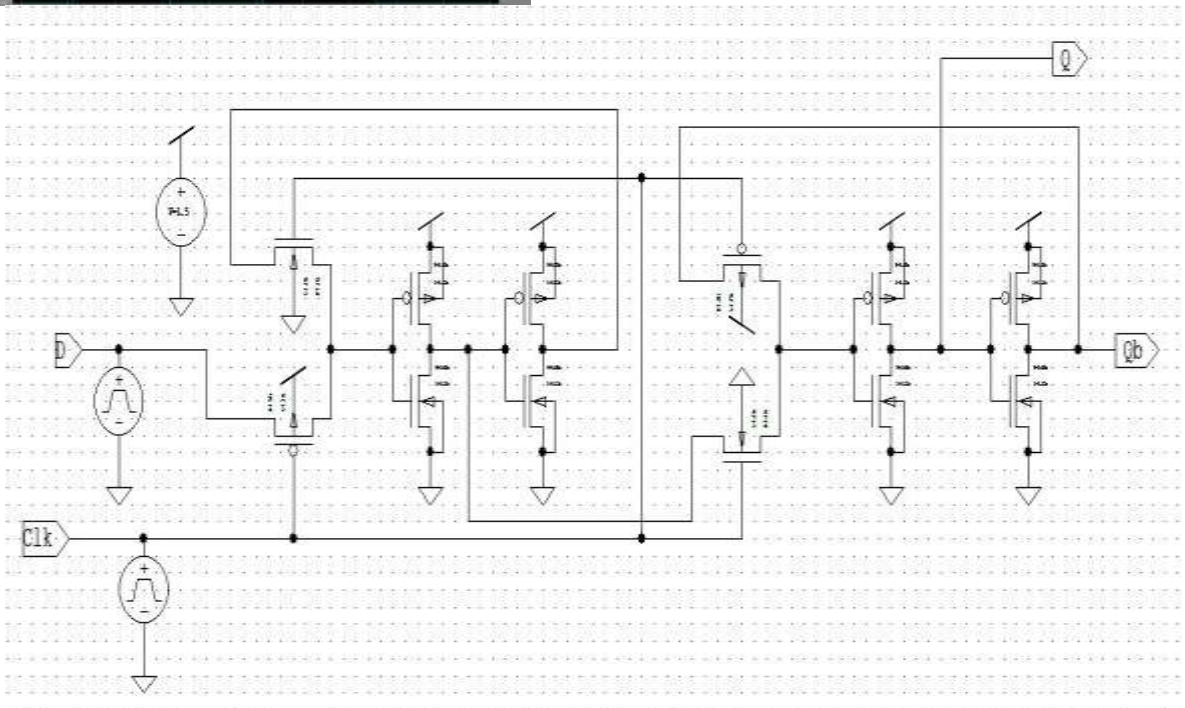

Fig. 8: GDI MUX DFF

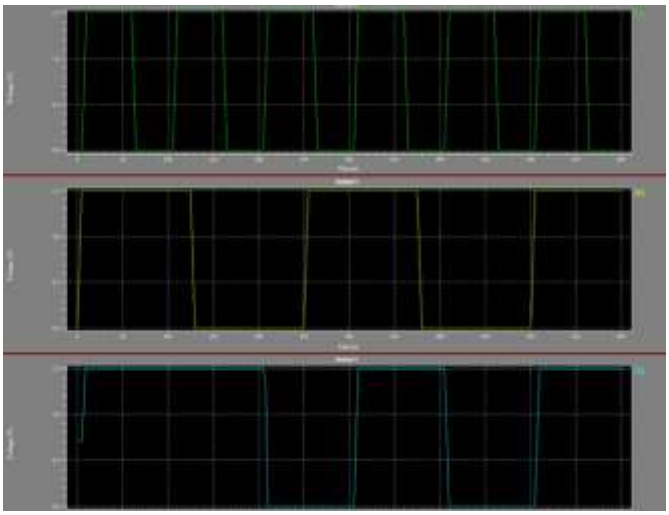

Fig. 9: Output Waveform of GDI MUX DFF

E. TG (Transmission Gate) D Flip Flop

A CMOS Transmission gate can be constructed by Parallel combination of NMOS and PMOS transistors. With complementary gate signals, the symbol of transmission gate is shown in figure 10. And the circuit of TG DFF is shown in figure.11.

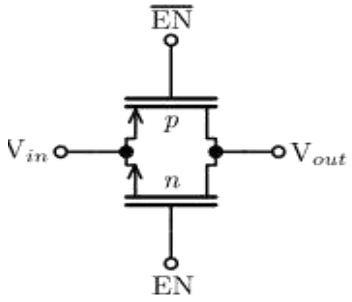

Fig. 10: Symbol of Transmission gate

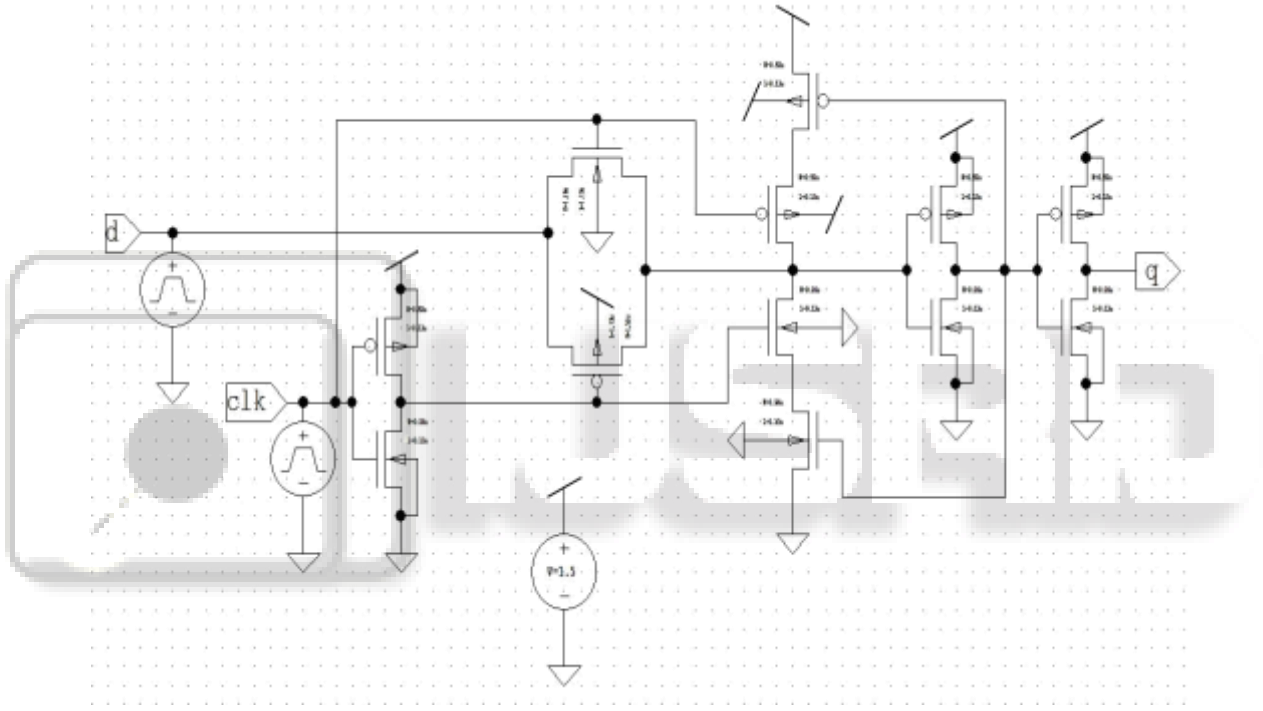

Fig. 11: TG DFF

The main advantage of Transmission gate compared to NMOS transmission gate is to allow the input signal to be transmitted to the output without the threshold attenuation. The output waveform of TG D flip flop is shown in fig.12.

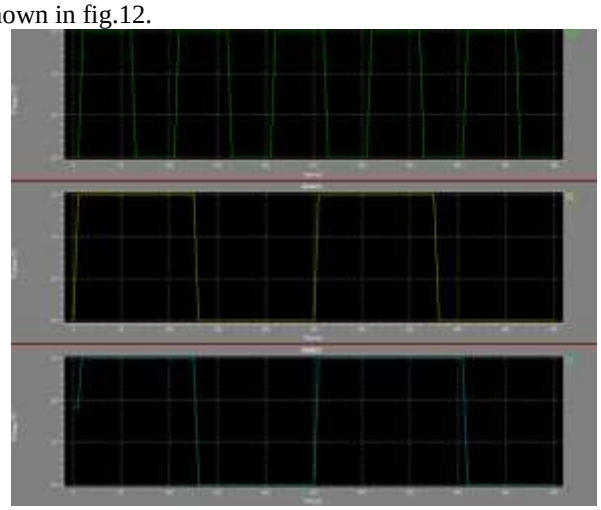

Fig. 12: Output waveform of TG DFF

F. Power PC D Flip Flop

Power Pc means performance optimization with enhanced RISC performance computing. The power dissipation is low also having the clock to output clock delay.

Main advantages, of power pc are short direct path and low power feedback. The circuit of power pc D flip flop is shown in figure.13.

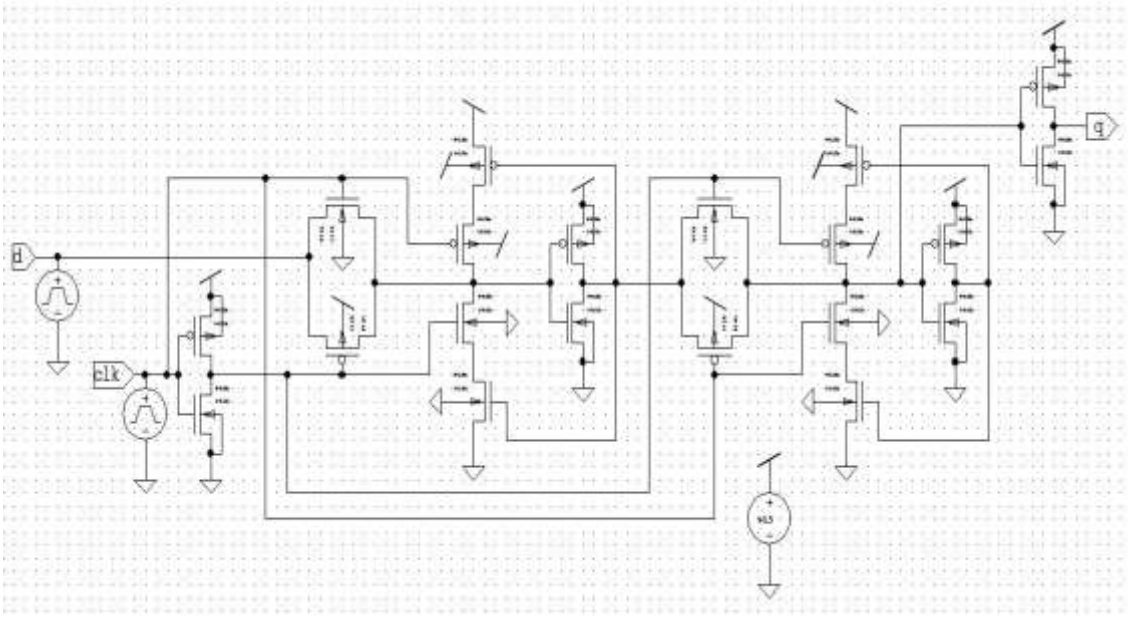

Fig. 13: POWER PC DFF

The output wave form of POWER PC D flip flop is shown in figure.14.

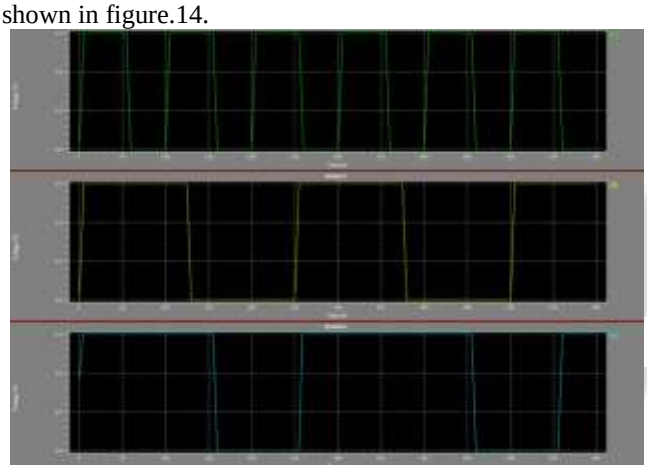

Fig. 14: Output waveform of POWER PC DFF

G. TSPC (True Single Phase Clocked) D Flip Flop

In this we have only clock and do not need an inverted clock. This technique is eliminated skew problems due to different cock phases .The TSPC logic style was introduced to overcome the complexity of the circuit. The circuit of TSPC D FF is shown in figure 15& Output waveform is shown in figure 16.

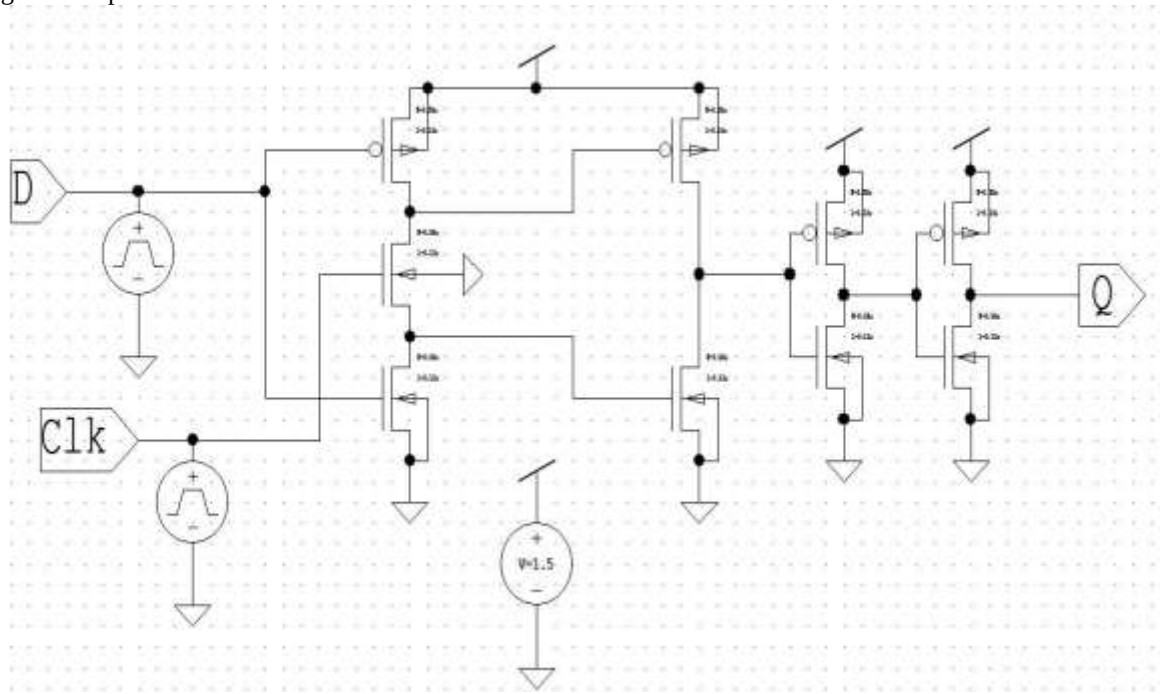

Fig. 15: TSPC DFF

The output waveform of TSPC D flip flop is shown in figure 16.

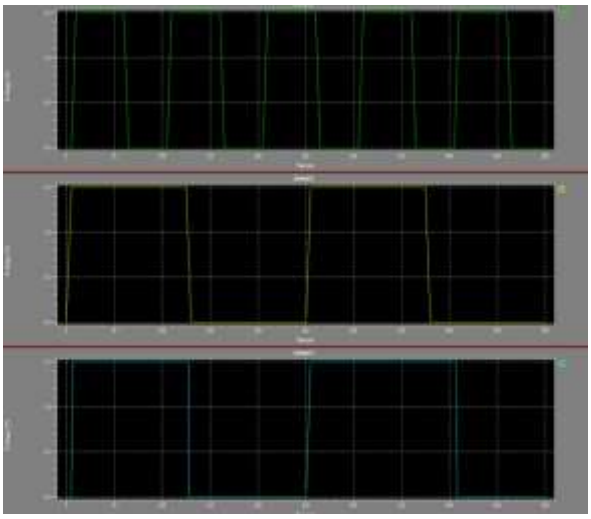

Fig. 16: Output waveform of TSPC DFF

The simulation results and comparison of these techniques is done using TANNER EDA at 180nm &130 nm technologies. The comparison of 180 nm is shown in Table 1 and comparison of 130nm is shown in Table.2.

In this 1.8 v used for 180nm technology and 1.3 v used for 130nm technology on 100 MHz frequency.The comparison is done on the basis of Transistor count ,power dissipation, propagation delay and figure of merit.

Design style	Power Dissipation (uw)	Propagation delay(ns)	Figure of merit	Transistor count
STATIC CMOS	3.2	4.93	15.78	18
CCMOS	0.94	4.71	4.43	14
GDI	1.06	55.48	58.81	18
GDI MUX	2.9	2.73	7.92	12
TG	1.06	4.67	4.95	12
POWER PC	58.14	30	1744.20	20
TSPC	0.77	0.37	0.28	9

Table 1: Comparison at 180nm Technology

Design style	Power Dissipation (uw)	Propagation delay(ns)	Figure of merit	Transistor count
STATIC CMOS	2	4.94	9.88	18
CCMOS	0.52	4.71	2.4492	14
GDI	1.3	55	71.5	18
GDI MUX	2.43	2.78	6.7554	12
TG	1.33	0.001	0.00133	12
POWER PC	0.09	30	2.7	20
TSPC	0.53	0.29	0.1537	9

Table 2: comparison at 130nm technology shown below:-

It is concluded from power dissipation comparison that power pc has lowest power dissipation at 130nm and TSPC at 180nm.and according to propogation delay comparison that TG design style has least propogation delay at 130nm and TSPC at 180nm.according to number of transistor count comparison TSPC has less number of transistors.

IV. Conclusion

It is concluded from comparison that TSPC & TG has best performance in terms of speed and, power dissipation at lower supply voltage. So it is better to use TG or TSPC logic style to design a system where fast speed is required. Thus electronics circuits with design TSPC logic style will occupy less space on chip.

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