Comparative Analysis of Comparators using Different Adder Styles at 180nm

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Abstract— In this paper 4-bit comparators are designed with six different logic of full-adder design styles at 180nm VLSI technology and all designs operated at 3.3Mhz frequency 1.8V that simulates all circuits. The circuits are designed and simulated using Tanner EDA software tools. It is concluded from power dissipation comparison that CMOS has lowest power dissipation results while DVL design style has highest in comparison. It is concluded from Propagation delay comparison that DPL design style has least propagation delay time at 180nm. So it is better to use DPL/DVL logic style to design a system where fast speed is required. The GDI and CPL technique have large delay compare to others. It is concluded from number of transistors comparison that TG technique requires less number of transistor to design a system than other two design styles. So electronics circuits designed using TG logic style will occupy less space on the chip. It is also concluded that TG style has the lowest figure of merit than other two design styles at 180nm. Thus TG and DVL have the best performance in terms of speed and power dissipation at lower supply voltages. It is a also concluded that as technology is scaling down, it is becoming more advantageous in terms of less supply voltages, less power dissipation and having less delay. Main emphasis on Power Delay Product which is less in Transmission gate logic style of adders.

Key words: 4-Bit Magnitude Comparator, PDP, Propagation Delay, Power Dissipation

I. INTRODUCTION

Comparator is a combinational circuit that compares two binary numbers and determine their relative magnitude and decides which number is greater , smaller or both are equal. Comparison between two binary numbers is widely used in computer systems, operational amplifiers and zero Crossing detector devices. Digital comparators are made up from standard AND, NOR and NOT gates that compare the digital signals present at their input terminals and produce an output depending upon the condition of inputs. Current comparator is fundamental component of analog system because of better accuracy, low noise and low power consumption. It can be used in A/D converters, oscillators, current to frequency converters, VLSI neural network, sensor circuit and portable wireless communication. Consider the simple 1-bit comparator below. In this, there are two inputs (A&B), and three outputs (C,D & E).

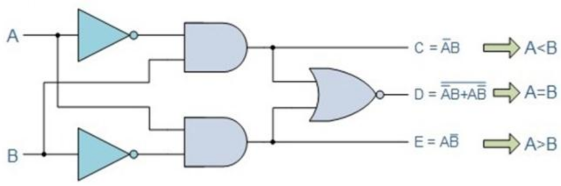

Fig. 1: Logical circuit diagram of 1-bit comparator

Inputs		Outputs		
B	A	A > B	A = B	A < B
0	0	0	1	0
0	1	1	0	0
1	0	0	0	1
1	1	0	1	0

Table 1: Truth Table of 1-Bit Comparator

A very good example of this is the 4-bit Magnitude Comparator. Here, two 4-bit words ("nibbles") are compared to each other to produce the relevant output with one word connected to inputs A and the other to be compared against connected to input B as shown below:

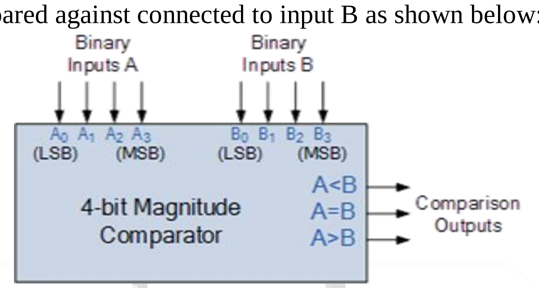

Fig 2: Basic block diagram of 4-bit comparator

II. 4-BIT COMPARATOR USING FULL-ADDERS

A. 4-Bit Comparator

The main building blocks of digital comparators are 1-bit (3 Ripple carry adders)full adder, AND gate and NOR gate as shown in figure below.

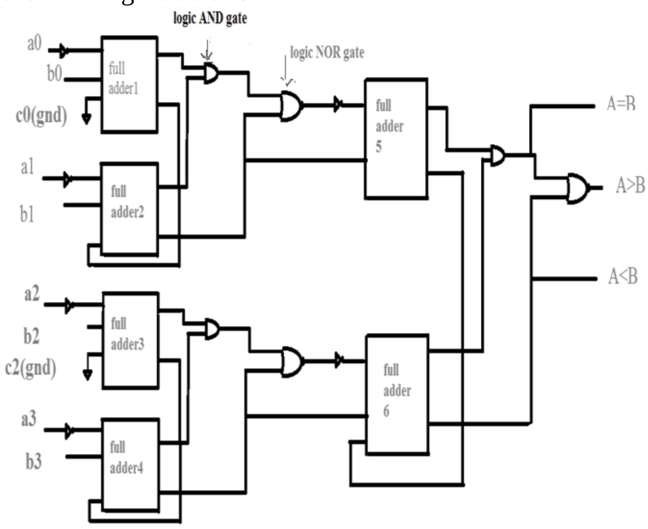

Fig. 2: Block Diagram of proposed circuit of 4-bit magnitude comparator

1) Conventional Static CMOS Logic (CSL)

Conventional static CMOS logic is used in most chip designs in VLSI applications. It consists of complementary nMOS pull-down and pMOS pull-up networks to drive '0' and '1' outputs.

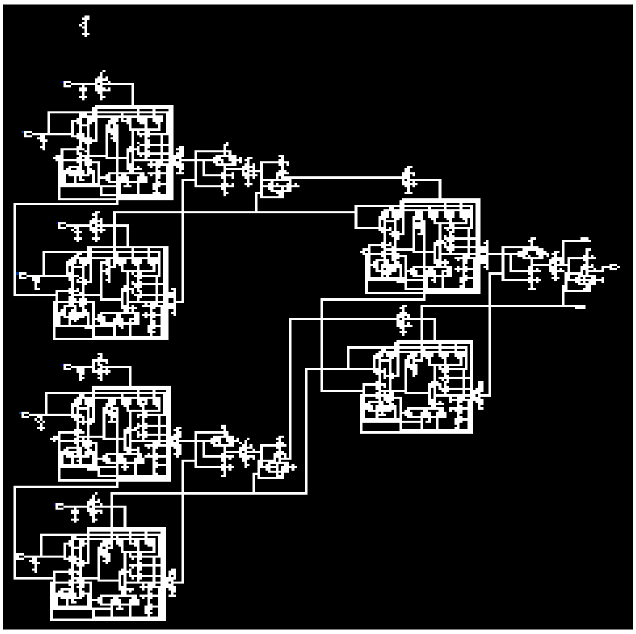

Fig. 3: Schematic Diagram of CSL 4-bit comparator

2) Complementary Pass-Transistor Logic (CPL)

This Logic Design Style has following advantages [30]:

- It belongs to the class of static gates, because the output-defining nodes are always connected to either V_{dd} or GND through a low resistance path.
- The design is modular. All gates use the same topology, only inputs are permuted. This makes design of a library of gates very simple.
- The availability of both polarities of every signal eliminates the need for extra inverters.
- Less number of transistor as pMOS transistors are eliminated.

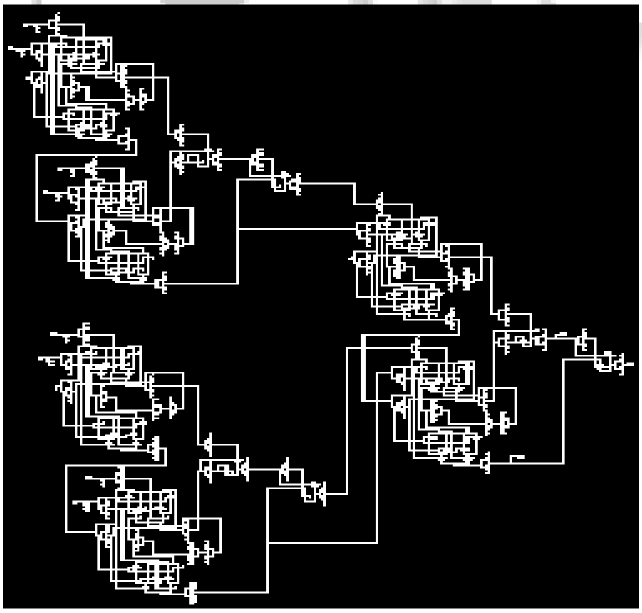

Fig. 4: Schematic Diagram of CPL 4-bit magnitude comparator

3) Double Pass Transistor Logic (DPL)

The Double Pass transistor logic is a modified version of CPL. The DPL also has complimentary inputs and outputs and thus it is implemented using dual-rails. In DPL circuits, full voltage swing is achieved at outputs by adding a pMOS transistor in parallel with nMOS transistors.

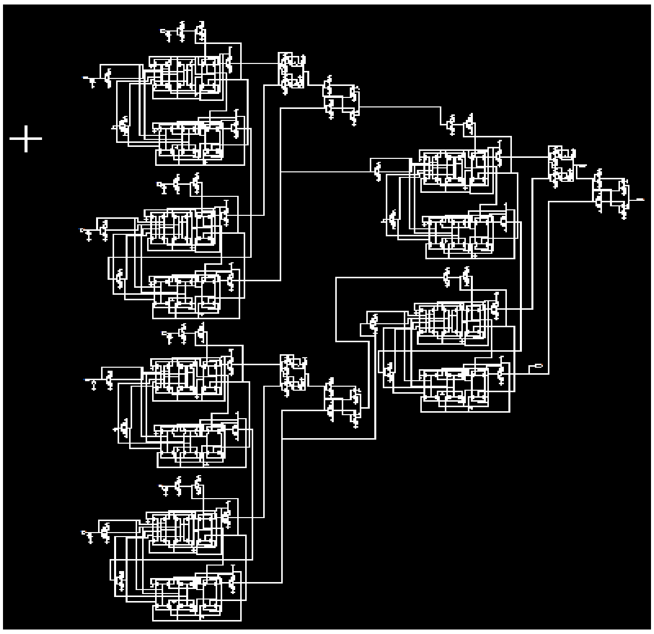

Fig. 5: Schematic Diagram of DPL 4-bit comparator

4) Transmission Gate Logic (TG)

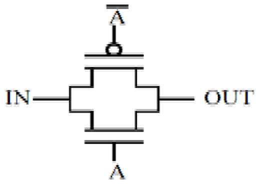

Fig. 6: A Transmission Gate Symbol

TG exhibits better speed and less power dissipation than the conventional CMOS due to the small transistor stack height.TG circuits have least number of transistors and no complementary input signals are required.

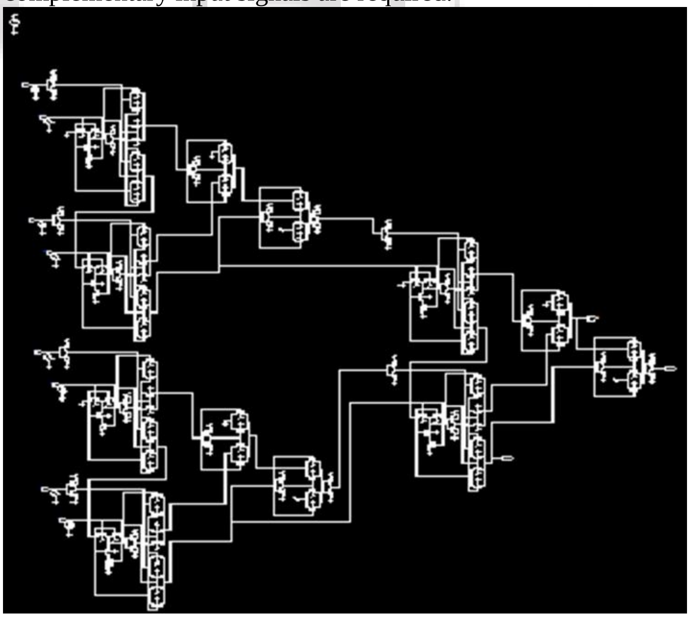

Fig. 6: Schematic diagram of TG 4-bit magnitude comparator

5) Gate Diffusion Input Logic (GDI)

a) Advantages of GDI Logic Style

GDI requires least number of transistors to implement circuits and acquired small area as compared to other design styles. GDI has least static power dissipation as compared to CMOS and other logic styles. It reduced dynamic component of power consumption as source of p-MOS is not tied to Vdd permanently.

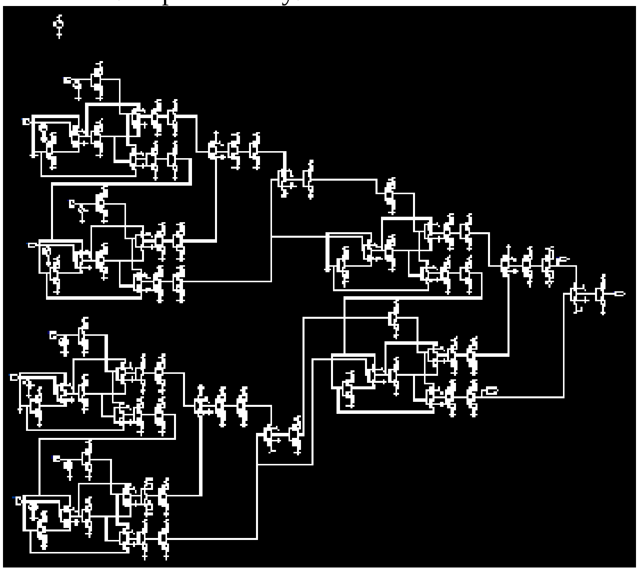

Fig. 7:Schematic diagram of TG 4bit magnitude comparator

III. CMOS DESIGN GOALS

Here two parameters affect the CMOS design:

- Power dissipation
- Delay in CMOS Circuits

A. Power Dissipation in CMOS Circuits

The average power dissipation in CMOS circuits can be expressed as the sum of three main components, namely, (1) the static power dissipation, (2) the dynamic (switching) power dissipation, and (3) the short circuit power dissipation [32].

1) Static Power Dissipation

Static Power Dissipation within CMOS circuit is due to leakage current between gate and substrate and current between drain and source. The reverse diode leakage occurs when the p-n junction between the drain and the bulk of the transistor is reversely biased. The reverse-biased drain junction then conducts a reverse saturation current which is eventually drawn from the power supply. A similar situation can be observed when the input voltage is equal to zero, and the output voltage is charged up to V_{DD} through the pMOS transistor. Then, the reverse potential difference between the nMOS drain region and the p-type substrate causes a reverse leakage current which is also drawn from the power supply (through the pMOS transistor). The magnitude of the reverse leakage current of a p-n junction is given by the following expression:

$$I_{rev} = A.J_s\left(e^{qV_b/kT} - 1\right) \qquad (1.1)$$

where 'V_b' is the magnitude of the reverse bias voltage across the junction, 'J_S' is the reverse saturation current density, 'A' is the junction area, 'k' is the Boltzmann's constant and 'T' is the temperature in Kelvin. Static power dissipation is given by:

$$P_s = I_{rev}.\text{Supply Voltage}.n \qquad (1.2)$$

where 'n' is the no. of devices. As MOSFET technology advances, the need for smaller MOSFET requires components such as a gate width or insulator width to be correspondingly reduced.

2) Dynamic Power Dissipation

In CMOS circuits, dynamic power is dissipated when energy is drawn from the power supply to charge up the output node capacitance. The dynamic power of a CMOS circuit is calculated using the equation:

$$P_{dyn} = C_L.V_{DD}^2.a.f \qquad (1.3)$$

Where 'f' is the operating frequency of the CMOS circuit, 'VDD' is the supply voltage of the circuit, 'a' is the switching activity of the CMOS gate and 'CL' is the average gate load capacitance.

3) Short Circuit Power Dissipation

The final and smallest component of CMOS power is the short circuit dissipation seen during CMOS transition.

$$P_{sc} = I_{mean}.V_{DD} \qquad (1.4)$$

B. Delay in CMOS Circuits

Logic delay through a gate is called propagation delay time. It is the average time needed for the output to respond to a change in the input logic state. The 't_{PLH}' defines the response time of the gate for a low to high (or positive) output transition, while 't_{PHL}' refers to a high to low (or negative) transition.

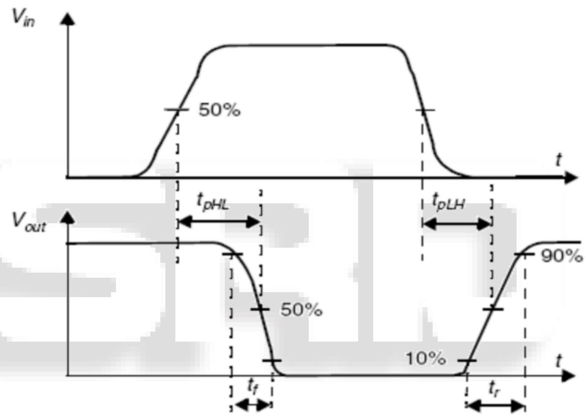

Fig. 8: Definition of propagation delay, rise and fall times [RCN03]

The propagation delay 'τ_p' is defined as follows:

$$\tau_p = \frac{t_{PLH} + t_{PHL}}{2} \qquad (1.5)$$

The propagation delay is not only a function of the circuit technology and topolog

IV. OBJECTIVE OF THE PAPER

The motivation behind VLSI is lower cost, higher speeds, higher reliability and shorter design times. Basically area and speed are main design goals but today power consumption has also become a critical concern. To minimize the power consumption for any digital system needs design optimization that includes technology used to implement the digital circuits, the circuit style and topology. Comparator is such an important element which contributes substantially to the total power consumption of the system [21]. On VLSI level, the area also becomes quite important as more area means more system cost. Smaller area of multiplier results in less switching capacitance and low power consumption [22][23]. In this paper CSL,CPL, DPL, DVL, GDI and TG design styles are used in design of 4-bit comparator at 180nm and 90nm technology. After that comparison of these six different logic styles is done in terms of area, delay and power dissipation.

V. Performance Analysis of Different Design Style

Design Style	Power Dissipation (μW)	Propagation Delay (nsec)	Figure of Merit (μ-nJ)	No. of Transistors
Length of Transistors used	AT 180nm	AT 180nm	AT 180nm	AT 180nm
CMOS	2.69	0.42	1.12	210
CPL	27.64	1.17	32.34	210
DPL	4.50	0.36	1.61	264
GDI	35.02	1.42	49.73	150
TG	8.00	0.11	0.90	138

Table 2: Performance Parameters of different design styles of Comparators

VI. Future Scope of Work

Future work in this thesis may include a further scaling down of the technology. Hybrid comparators architecture which is a mixture of design styles can be advised so that speed can be increased and power dissipation can be decreased at decreased channel length.

References

[1] Raja Mohd. Noor, Hafizi Raja Daud, Mamun Bin Ibne Reaz and Labonnah Farzana Rahman, "Design and Analysis of Low Power and High Speed Dynamic Latch Comparator in 0.18 µm CMOS Process", International Journal of Information and Electronics Engineering, Volume. 2, No. 6, November 2012

[2] Neeraj K. Chasta, "High Speed, Low Power Current Comparators with Hysteresis", International Journal of VLSI design & Communication Systems (VLSICS), Volume 3, No.1, February 2012

[3] Geetanjali Sharma, Uma Nirmal and Yogesh Misra, "A Low Power 8-bit Magnitude Comparator with Small Transistor Count using Hybrid PTL/CMOS Logic", International Journal of Computational Engineering & Management, Volume 12, April 2011

[4] D.Nageshwar Rao, M.S Sameera, M D.Nizamuddin Salman and Zubeda Begum, "Design of Low Power High Speed Fully Dynamic CMOS Latched Comparator", International Journal of Engineering Research and Development, Volume 10, Issue 4, April 2014

[5] Dinabandhu nath Mandal, Niladri Prasad Mohapatra, Rajendra Prasad and Ambika Singh, "Analysis and Design of Low Voltage Low Power Dynamic Comparator with Reduced Delay and Power", International Journal of Engineering Research and General Science, Volume 2, Issue 3, April-May 2014

[6] Shruti Hathwalia, "Analysis & Design of Low Power CMOS Comparator at 90nm Technology", International Journal of Engineering Research and Applications, Volume 4, pp.289-292, April 2014

[7] Eric R. Menendez, Dumezie K. Maduikez, Rajesh Garg and Sunil P. Khatri, "CMOS Comparators for High-Speed and Low-Power Applications", IEEE, 2006

[8] Fernando Paixao Cortes, Eric Fabris and Sergio Bampi, "Analysis and design of amplifiers and comparators in CMOS 0.35 nm technology", Microelectronics Reliability, Volume 44, pp. 657–664, 2004

[9] Monica Rose Joy and Thangamani M., "Design and Analysis of Low Power Comparator Using Switching Transistors", Volume 4, Issue 2, pp. 25-30,April 2014.

[10] Abhishek Rai and Ananda Venkatesan, "Analysis and Design of High Speed Low Power Comparator in ADC", International Journal of Engineering Development and Research, Volume 2, Issue 1, 2014

[11] N. Naga Sudha, V. Narasimha Nayak, Suneel Mudunuru, M. Nagesh Babu and M. Jyothi, "High Speed and Low Power Dynamic Latched Comparator for PTL Circuit applications", International Journal of Computer Science and Information Technologies, Volume 3, pp. 2982 – 2991, 2012

[12] Jaeha Kim, Brian S. Leibowitz, Jihong Ren and Chris J. Madden, "Simulation and Analysis of Random Decision Errors in Clocked Comparators", IEEE Transactions on Circuits and Systems, Volume 56, No. 8, August 2009

[13] Vinotha V and Menakadevi B, "Design of Low-Voltage, Power Proposed Dynamic Clocked Comparator", International Journal of Engineering Science and Innovative Technology, Volume 3, Issue 1, January 2014

[14] R Zimmermann and W Fichtner, "Low power logic styles : CMOS versus Pass Transistor Logic", IEEE Journal of Solid-State Circuits, Vol. 32, No. 7, pp. 1079-1090, July 1997.

[15] C Nagendra and M J Irwin, "Design tradeoffs in CMOS FIR filters", International Conference on Acoustics, Speech & Signal Processing, Vol. 6, pp. 3260-3263, 1996.

[16] Pouya Asadi and Keivan Navi, "A novel high - speed 54 × 54 bit Multiplier", American Journal of Applied Sciences, pp. 666-672, 2007.

[17] Zhijun Huang and Milos D Ercegovac, "High Performance Left-to-Right Array Multiplier Design", 16th IEEE Symposium on Computer Arithmetic, pp. 4, 2003.

[18] www.mosis.com

[19] G Moore, "Cramming more Components into Integrated Circuits", Electronics, Vol. 38, No. 8, April 1965.

[20] Sung Mo Kang and Yusuf Leblebici, "CMOS Digital Integrated Circuits" , Third Edition, Tata McGraw Hill Publisher, 2003.

[21] Azeez J Bhavnagarwala, Ashok Kapoor and James D Meindl, "Dynamic-Threshold CMOS SRAM Cells for Fast, Portable Applications", ASIC/SOC Conference, 2000.

[22] F Faggin et al., " The MCS-4 An LSI Microcomputer System", 1972 IEEE Region Six Conference Record, San Diego, pp. 1- 6, April 1972.

[23] Michael J Riezeman, "Wanlass's CMOS Circuit", IEEE Spectrum, pp. 44, May 1991.

[24] Jan M Rabaey, Anantha Chandrakasan and Borivoje Nikolic, "Digital Integrated Circuits", Second Edition, PHI Publishers, 2003.

[25] N H E Weste and D Harris, "CMOS VLSI Design: A Circuits and Systems Perspective",3rd International Edition, Addison-Wesley, 2004.

[26] A P Chandrakasan and R W Brodersen, "Low Power Digital CMOS Design", Norwell, Kluwer Academic Publishers, 1995.

[27] Sharma, A.Sharma,"Area and power efficient 4-bit comparator design by using 1-bit fulladder module "Parallel, Distributed and Grid Computing (PDGC), 2014 International Conference on DOI: 10.1109/PDGC.2014.7030705 Publication Year: 2014 , Page(s): 1 – 6.

