Design of Low Power Asynchronous Viterbi Decoder for Wireless Communication

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Abstract— Convolutional codes are mainly used in channel coding techniques, and because of high performance, Viterbi decoder is widely used in decoders. Also fast developments in communication field have created rising demand for low power, high speed and low weight Viterbi decoders. Though there is significant growth in past few years but still problem of power dissipation in Viterbi decoders remained challenge and requires further technical solution. The aim of this project is to reduce the dynamic power consumption below 10 mW Asynchronous Technique is a technique where handshaking signal are used to communicate between blocks. The asynchronous design is inherently data driven and active while doing useful work where power saving with acceptable speed penalty is obtained. Xpower analyzer tool is used to measure power consumption. Therefore, the designed method is of low power consumption of Viterbi decoder for the rate of r=1/2, with a constraint length K = 3 using asynchronous technique.

Key words: VHDL, Asynchronous Viterbi decoder

I. INTRODUCTION

This chapter will give brief introduction to Convolutional (Viterbi) decoding. It is a Forward Error Correction (FEC) technique [1]. The Motto of this is to improve the capacity of channel by adding some carefully designed inessential information to the data which is transmitted from the channel. The process of inserting this needles information is known as channel coding. For this purpose we are using two main forms of channel coding techniques which is convolutional coding and block coding. In Convolutional coding data operates serially, one or a few bits at a time. Block codes are operated on large message blocks typically hundreds of bytes. There is a variety of block codes and convolution codes, and a variety of algorithms are used for decoding the received coded information sequences to get back the original data.

A. Convolution Encoder

The Convolutional encoder is similar to finite state machine. It gives coded output for input data. It is usually made up of network of XOR (Exclusive-OR) gates and shift registers as shown in Fig. 1.1 for every single input bit it generates two bits of coded output Therefore it is called as ½ rate encoder. A Convolutional encoder is generally characterized in (n, k, m) format, where k is number of inputs to the encoder; m is number of Flip Flop used (memory elements) of the longest shift register of the encoder and n is number of outputs of the encoder. The encoder shown in the figure is a (2, 1, 2) encoder with rate 1/2.

Fig. 1: Convolutional Encoder with rate=1/2 and Constraint length=3

B. Viterbi Decoder

Viterbi decoders are widely used in digital communication for transmission and is expected to be used in next generation wireless communication. A Viterbi decoder at the receiver side uses the Viterbi algorithm for decoding a received bit stream that has been encoded using a convolutional code at transmitter side. Two design styles are available for the implementation of Processors, synchronous and asynchronous. Conventional synchronous processor designs are controlled by a global clock, it runs continuously from starting of the process. Asynchronous designs are locally synchronized rather than globally and use handshaking signals between their internal components for necessary local synchronization and to sequence the events of process. There are many advantages for asynchronous design technique rather than synchronous techniques. Synchronous techniques involves higher switching because of which it dissipates large amount of power. But asynchronous techniques has less amount of switching and hence dissipates less amount of power. High switching activity translates into a large amount of wasted power. In asynchronous technique idle part consumes negligible power and switching activity is depends only with useful work being done which is an important feature for battery operated devices.

Fig. 2: Viterbi Decoder Block Diagram

In Viterbi decoder LIFO unit is combined with predictor unit and this predictor and LIFO unit is covered in Fast trace unit in design flow fig 3.
II. DESIGN METHODOLOGY
The Design Methodology Viterbi decoding algorithm given below it consists of various steps to find the decoded data. In this, a Convolutional encoder generate the code using VHDL, for every single bit it generates two bits of coded output which is pass as input to the Branch Metric unit(BMU), it finds out the hamming distance by comparing bit by bit using adder circuit and the output is represented in two bits. The output of BMU send to Add Compare Select unit (ACSU) as a input, it adds and compare the data. The output of ACS unit is of four bit including one select line. The shortest path is selected. The output of ACSU given to memory unit to store and process the data in register and the process data pass to the output unit to maintain data on its stack register all the procedure it will generate the output. In register exchange method Last in First out unit in not required but in trace back method Last in First Out is needed. The decoded bits are placed in reverse order to make it straight LIFO is needed. In proposed system trace back technic is used therefore LIFO unit is needed in circuit. Controller block is used to maintain the handshaking signals for asynchronous communication. Controller block maintains the asynchronous communication which then activates the few blocks at a time which is needed for the continuation of process. Because of which power dissipation will reduce.

![Fig. 3: Design Flow of Viterbi Decoder](image)

A. BMU & ACS Combined Block
The BMU and ACS Combined block does the work of both, it calculates the hamming distance between the two inputs. The input data is of two bits each. Then it adds the data of path matrix and branch matrix then comparison is done. After that shortest path is get selected and S3 signal shows the status that which path is selected for transmission. The state matrix have to be updated at every cycle of clock. Hence it consumed maximum power.

![Fig. 4: BMU and ACS Combined Block](image)

As shown in fig above if rin = 01 & ro=11 then xor is 10 and number of count is 01. Addition of 01 with PM0 = 10 is 011. Similarly for rin = 01 , r1 = 10 and PM1= 10 adder output is 100. The shortest path between 011 and 100 is 011. Therefore output for 1st input trail is 011.

B. Memory
Almost all the memory is stored in Path Matrix (PM). The ACS unit is further sub divided into smaller blocks which decide the word length of the memory. In the proposed paper the code trellis length decides the depth of the memory to be used. Suppose that the constraint length is 3 bit i.e. K = 3 and output of each ACS block comprises of 4 bit then the memory block that can be used is 4x12 where 12 is the trellis length. The memory contains two different ports one for reading and another for writing. The main purpose of this dual port is to use different addresses for reading and writing. Write operation should be performed in synchronous nature whereas read operation should be performed in asynchronous manner. This is done to keep the delay also termed as transport delay in some cases, in check thus keeping the synchronous systems in harmony with the system behavior.

C. Predictor Unit
In context of a Viterbi decoder it is important to predict the next state thereby finding the actual decoded bit. This is carried out by a predictor unit in the decoder thereby tracing back the code trellis length. A state machine is used to identify a critical path with fastest time delivery. The state machine unit contains a value which helps in providing an access to the memory. This Unit is also called as Fast Trace Unit.

D. Last in First Out
In register exchange method Last in First out unit in not required but in trace back method Last in First Out is needed. The decoded bits are placed in reverse order to make it straight LIFO is needed. In proposed system trace back technic is used therefore LIFO unit is needed in circuit. The output of predictor unit is given to LIFO unit. In this system predictor unit and LIFO unit is combined. Therefore it is not mentioned differently in flow design and block diagram.

E. Controller
The system should work as a proper unit thus satisfying proper timing requirements. This is taken care of with the help of a Controller. A Controller has the responsibility to connect to all the sub units and modules at the same time. Synchronizations are required. The other important task of the controller includes counting which is carried out by an up counter and a down counter. Thus the addresses of memory to be read or written are driven by the counters.

III. TYPES OF VITERBI DECODING
In order to realize a certain coding scheme a suitable measure of similarity or distance metric between two code words is vital. The two important metrics used to measure the distance between two code words are the Hamming distance and Euclidian distance adopted by the decoder depending on the code scheme, required accuracy, channel characteristics and demodulator type. In proposed system hard coding is used because in HDL coding it is not possible to do quantization. It is possible in mixed signal analysis. HDL coding works on digital values 0 and 1. In proposed
system two bit error is introduced in channel to make sure that proposed system is working perfectly as Viterbi decoder because the main purpose of Viterbi is to detect and correct the error.

A. Hard Decision Viterbi Decoding

In the hard-decision decoding, the path through the trellis is determined using the Hamming distance measure. Thus, the most optimal path through the trellis is the path with the minimum Hamming distance. The Hamming distance can be defined as a number of bits that are different between the observed symbol at the decoder and the sent symbol from the encoder. Furthermore, the hard decision decoding applies one bit quantization on the received bits.

B. Soft Decision Viterbi Decoding

In the Viterbi Algorithm, there are two ways to calculate the distance to choose a most likelihood path. One is hamming distance which is related to the hard decision. The other one is Euclidean distance related with soft decision. Soft-decision decoding is applied for the maximum likelihood decoding, when the data is transmitted over the Gaussian channel. On the contrary to the hard decision decoding, the soft-decision decoding uses multi-bit quantization for the received bits, and Euclidean distance as a distance measure instead of the hamming distance. The demodulator input is now an analog waveform and is usually quantized into different levels in order to help the decoder decide more easily.

IV. RESULTS

A. Combination of BMU and ACS

<table>
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<th>R0</th>
<th>rin</th>
<th>R1</th>
<th>PM0</th>
<th>PM1</th>
<th>S3</th>
<th>o/p</th>
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<td>10</td>
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<td>10</td>
<td>11</td>
<td>01</td>
<td>1</td>
<td>010</td>
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</tbody>
</table>

Table 1: Combination of BMU and ACS

In combined block of ACS & BMU when we are giving 3rd input trail we get XOR output for r0 & rin is 10, count of 1 is 01. And for rin & r1 XOR is 10, count of 1 is 01. If these two outputs are added with PM output then adder output is 100 for PM0. And for PM1 we get 010. Finally the shortest path between these two outputs is 010. Hence S3 is 1 because 1st path is selected.

B. Encoder and decoder output

In proposed system Viterbi decoder is working perfectly. After 15 clock cycles output is coming after giving input to the encoder. The working of encoder and decoder is that the information given to the encoder should be collected at the decoder correctly. Error should be detected and corrected but the output should be same as input given to the encoder.

C. Power Result for the Complete Encoder and Decoder

In Proposed system objective is to reduce the dynamic power below 10 mW. In base paper that is “RTL Level Implementation of High Speed and Low Power Viterbi Encoder & Decoder” by Pooran Singh and Santosh Kr.Vishvakarma Dynamic Power given is 10.97 mW. So target is to reduce Dynamic power bellow 10 mW. In Xilinx it is not possible to get the dynamic power so .vcd file is created through modelsim. Then for every different input different dynamic power is occurred. So aggregate of all dynamic power is taken and approximate dynamic power for proposed circuit is achieved. In proposed system 3mW of dynamic power is achieved.

V. CONCLUSION

Viterbi decoders used in digital communications are very complex in designing and dissipate large amount of power. To overcome this difficulty, we are designing asynchronous Viterbi Decoder for Wireless Communication, because of asynchronous design is consumes less power because blocks are active only when doing useful work, and operate at the average speed of all components. Here this design have combined version of ACS and BMU unit. Using this circuit we have reduced 2 ACS blocks as compared to our first reference paper. Because of Low power dissipation battery backup will increase and Performance of the system will increase and system will survive for long duration. If we reduce dynamic power then static power is increasing. In proposed system hard coding is used rather than soft coding because HDL language cannot perform quantization. Quantization is possible in mixed signal analysis. Error is introduced in channel which is of two bits the maximum possible combination for two bit are four. After introducing error in channel this system is working efficiently and detecting and correcting the error successfully. The combined block of ACS and BMU unit is working perfectly after combining. And producing 4 bit data which is perfect according to the proposed working table for this circuit. In asynchronous design switching is reduced therefore dynamic power is reduced but area is increased. Because of which static power dissipation is increased. In Asynchronous technic because of hand shaking signal unit area increased.

REFERENCES


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