FPGA based Simulation of Clock Gated ALU Architecture with Multiplexed Logic Enable for Low Power Applications

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Abstract— Need of calculation based on hardware systems is increasing day by day. The performance of hardware directly effect the performance of hardware based applications and also the software applications whose execution is affected by hardware performance. So there is continuous need of the improvement in the hardware architectures to achieve a desired level of parametric and interface features. Arithmetic Logic Unit (ALU) is the most busy part of a system. Its performance is directly counted in analyzing the overall system performance. Due to highest activeness of ALU in a system so high performance architecture of an ALU is always desired in a design system. The performance of ALU is, now days, desired to be power efficient to make overall system power efficient and portable. In the presented work a 64-bit architecture of ALU is proposed with gated-clock control logic. The proposed logic design is a low power architecture of ALU. The work is simulated and synthesized using Xilinx ISE Design Tool and the results are tabulated in this paper.

Key words: Arithmetic Logic Unit, Clock Gating, Field Programmable Gate Array, Low Power Architecture, Opcode, Oprand, Xilinx ISE

I. INTRODUCTION

Processing of signals in integrated circuit at a high speed is required by the present system. This is because of the increase in the data that is to be handled by the systems. Due to a rapid rise in the application gadgets, software based applications and improved communication technologies, the amount of data has shown a rapid rise in the data communication and processing. A high speed communication link requires a high speed hardware to effectively manage the data during communication. And, when the system is such that there is requirement of real-time processing of data then the processing hardware should also be at par with the speed compatibilities of all the interfaces. An increase in the processing requirement of the system is directly related to the power consumption by the system. So, low power consumption is another parametric requirement of high data processing systems to maintain the overall performance of the system. A processing circuit is basically a logic design with logic execution unit and control logic. The controller enables the data synchronization with the interfaces and the logic execution unit handles the data to produce the desired output from the available inputs and controls. This logic execution unit is also called as Arithmetic Logic unit (ALU) in the cases where the data is processed or handled using arithmetic and logical operations. The performance of processing unit can thus be analyzed only by the performance of the control unit and the arithmetic logic unit. A block diagram of general processing unit is shown in Fig-1. ALU is also called as the Heart of any operating system. It is the hardware logic part of the system output from which is transferred to the other parts of the processing unit. The speed of hardware is also related to the speed of logic performance unit. The functions of ALU are not a fixed set of logical operations. An ALU may have any number of single-clock and multiple-clock operational blocks. The execution of these blocks is controlled using the controller unit. Many designs of processors, ALUs and intermittent operational units are proposed in previous works. The basic of Gate, Logical and Arithmetic operations are explained in reference [1]-[4]. Clock-gating technique for low-power design is implemented in references [5]-[8]. Clock-Gating based ALU architectures are proposed in [9]-[12]. Explanation of intermittent logics and architectures along with the hardware description language basics is referred from references mentioned in [13]-[19]. In the proposed work gated-clock ALU with multiplexed logic Enable architecture is presented. The rest of the paper description is arranged as: Section-2 explains the proposed architecture and its feature, Section-3 gives the Simulation results and the conclusion of the proposed work. The last part lists the references.

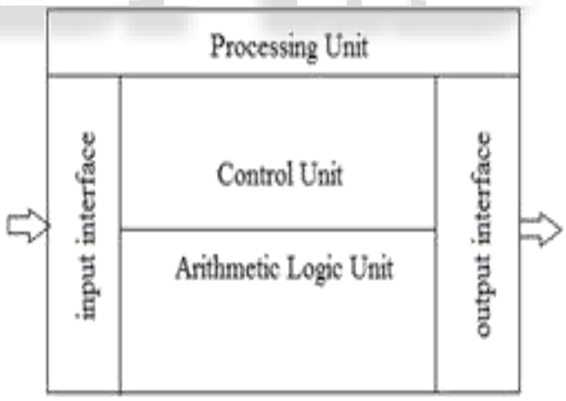

Fig. 1: Block Diagram of General Processing Unit

II. ALU ARCHITECTURE PROPOSED DESIGN

The design of proposed ALU is based on low power architecture. The low power constraint is achieved using clock-gating technique. In clock-gating method of hardware implementation the execution of sequential hardware is controlled using an additional hardware circuit that controls the flow of clock signal throughout the sequential hardware.

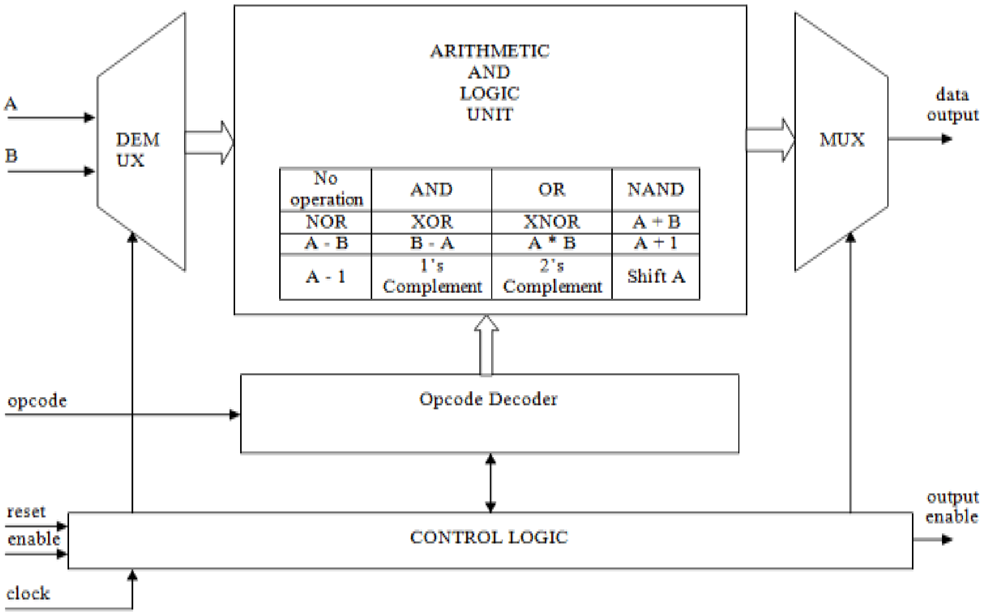

Fig. 2: RTL Block of Proposed ALU

This clock control hardware allows the flow of clock signal only for the time duration of the operational execution. This clock control hardware is sometimes referred as clock-gating logic unit. Since the sequential logic hardware does not receive the clock signal in the duration when the operational changes are not required, thus, avoiding the transition of hardware components. This saves the dynamic power consumption of the clock-gated hardware. The clock gating can also be applied on combinational logic hardware. In the proposed work, the operation of the ALU is controlled using clock-gating technique. The logical and arithmetic operations that are proposed in this work are listed in Table-1. Fig-2 shows the RTL block diagram of the proposed architecture. The data inputs 'A' and 'B' are transferred through demultiplexer hardware that enables the output into a particular operational block that is based on the value of 'opcode'. Similar logic with the help of a multiplexer logic is used to select the output of the performed operation. The data selection by the multiplexer is controlled by the 'opcode' input. To enable a particular operational block for operational execution an enable control signal is generated by the "opcode decoder" logic unit by decoding the 'opcode' input. A master 'reset' input is used to initialize all the registers of the propsed logic hardware to low logic value. An 'enable' input control is used to invoke the execution of the logic operation. The 'enable' input is also used to control the flow of clock signal in the hardware circuit with the help of clock-gating logic unit. In the proposed design the simulation of all the operations are performed on 64-bit values of input 'A' and 'B', except the multiplication operation. The multiplication operation can be performed only on 32-bit values of 'A' and 'B'. This is because the maximum value of the output of multiplication of two 32-bit numbers can be represented using 64-bit output. An 'output enable' is also used to indicate the availability of output of the execution of operation at the data output port. This output is used to synchronize the output with interface execution blocks.

Operation	Opcode Value
No Operation	0000
AND	0001
NAND	0010
OR	0011
NOR	0100
XOR	0101
XNOR	0110
Addition (A + B)	0111
Subtraction (A – B)	1000
Subtraction (B – A)	1001
Multiplication (A * B)	1010
Increment A	1011
Decrement A	1100
1's complement of A	1101
2's complement of A	1110
Shift A	1111

Table 1: Operation-Opcode Summary

III. CONCLUSION AND SIMULATION RESULTS

The simulation of proposed ALU logic is performed using Verilog HDL on Xilinx ISE version 13.3. The proposed design RTL block and Schematic are respectively shown in Fig-3 and Fig-4. The functional simulation results of proposed design for different logic operations are shown in Fig-5 to Fig-8. The input and output vectors values that are used for the functional simulation are mentioned as follows:

1) Simulation case-1 (Fig-5):

Opcode = 4'b0001 (AND Operation)
Operand A = 64'haaaaa00000000000
Operand B = 64'h7777700000000000
Result = 64'h2222200000000000

2) Simulation case-2 (Fig-6):

Opcode = 4'b1011 (Increment A Operation)

Operand A = 64'h6600000660002222
Operand B = 64'h3300077000001234
Result = 64'h6600000660002223

3) Simulation case-3 (Fig-7):
Opcode = 4'b0111 (Addition Operation)
Operand A = 64'h4400000000004321
Operand B = 64'h3300000000001234
Result = 64'h7700000000005555

4) Simulation case-4 (Fig-8):
Opcode = 4'b1001 (Subtraction (B-A) Operation)
Operand A = 64'h7000001111000000
Operand B = 64'h7000003333000000
Result = 64'h0000002222000000

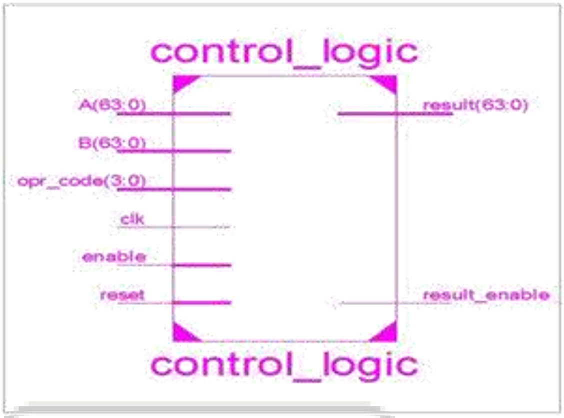

Fig. 3: RTL Block of Proposed ALU

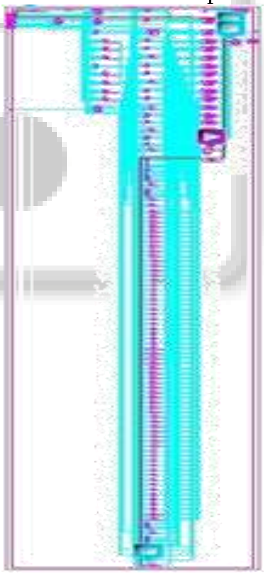

Fig. 4: RTL Schematic of Proposed ALU

The logic design simulation is performed on Xilinx Spartan3E XC3S500E-4FG320 FPGA. The hardware resource utilization summary is shown in Table-2.

Hardware Resource	Available	Utilized	Utilization %
Slices	4656	811	17%
Slice Flipflops	9312	137	1%
4-input LUTs	9312	1612	17%

Table 2: Hardware Resource Utilization Summary

The power performance of the proposed logic design is performed using Xilinx X-Power Tool. The Dynamic Power consumption versus Operational Clock Frequency is summarized in Table-3.

Frequency (MHz)	Dynamic Power (mWatt)
500	0.048
600	0.058
700	0.068
800	0.078
900	0.087
1000	0.097
1100	0.107
1200	0.116
1300	0.126
1400	0.136
1500	0.145

Table 3: Clock Frequency Vs Dynamic Power Consumption

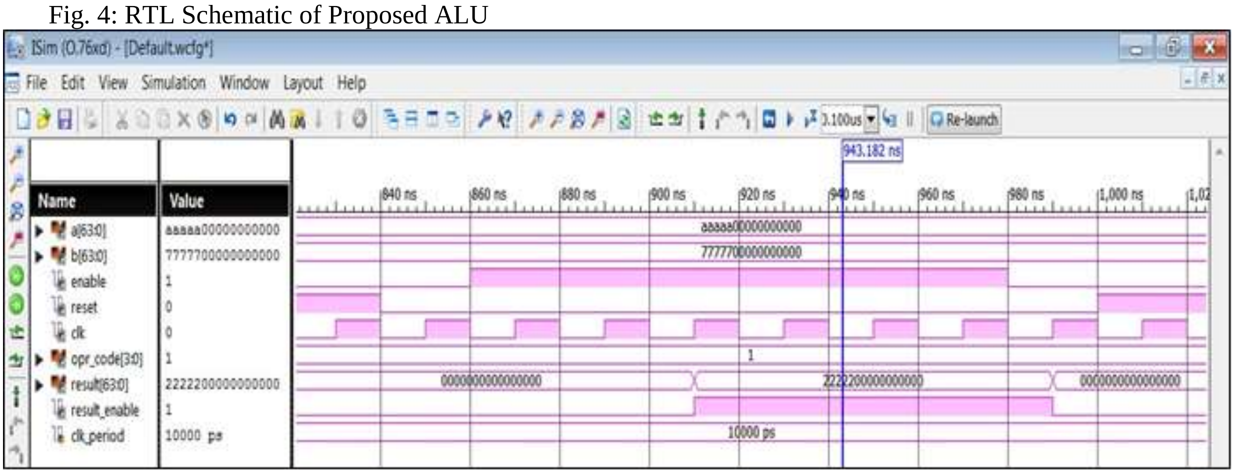

Fig. 5: Simulation waveform (AND Operation)

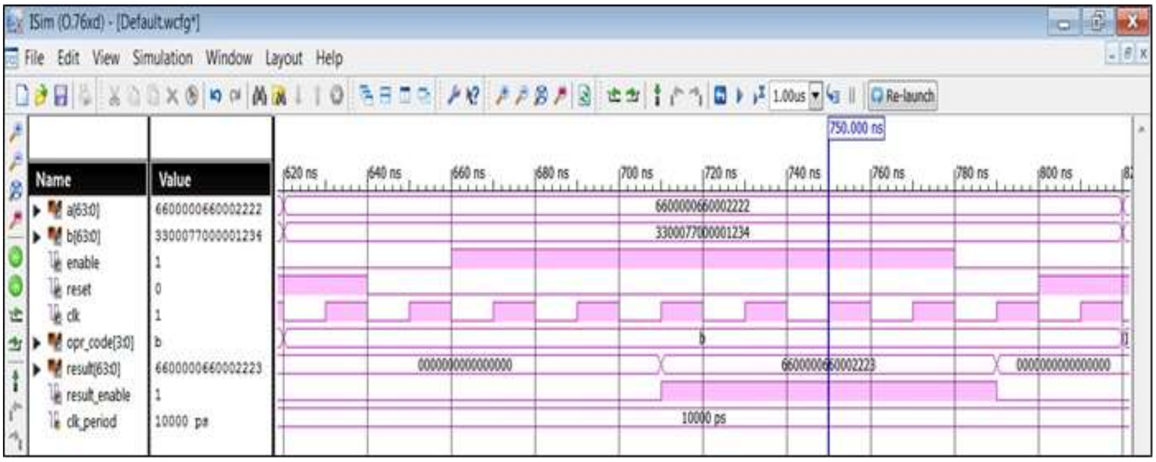

Fig. 6: Simulation waveform (Increment-A [A+1] Operation)

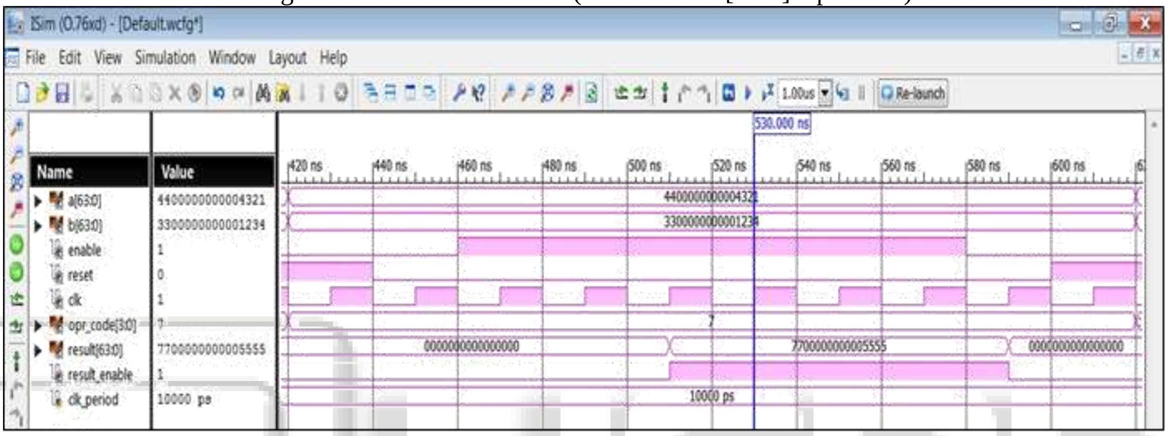

Fig.7: Simulation waveform (Addition [A+B] Operation)

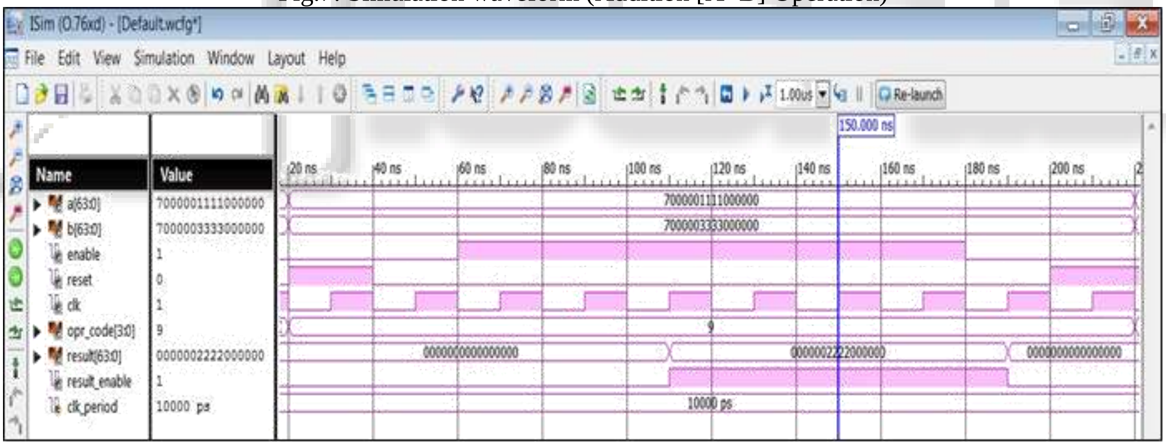

Fig. 8: Simulation waveform (Subtraction [B-A] Operation)

The presented work proposed a low power Gated-clock ALU architecture design. FPGA based simulation and synthesis results are presented as the output of the proposed work. This design gives an option for the common logic implementation of processing and calculation based logic designs. A 64-bit design is also good option for implementation of high precision operation processing and control systems. The low power architecture using Gated-clock offers a power based parametric advantage of proposed design for FPGA based design systems. The proposed work can be combined with other configurable design architectures for application specific integrated circuit implementation in future. In future, the proposed work can also be added with the built-in-self-test (BIST) capability to improve the design performance against hardware and functional failures.

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