Power Quality Improvement by Using Voltage Controlled DSTATCOM

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Abstract— In this paper a new algorithm is proposed for a DSTATCOM operating in voltage control mode to generate reference voltage. The proposed scheme enables that unity power factor (UPF) is accomplished at the load terminal in the nominal mode of operation, which is impractical in the traditional method. The compensator here is also used to inject lower currents so that the losses in the feeder and VSI are reduced. Further rating of DSTATCOM can also be reduced so that it mitigates the voltage sag. Nearly UPF can be maintained at the load terminal during load change. Due to the above reasons the DSTATCOM increases the power quality by improving power factor, harmonic reduction, and tight voltage regulation. Simulation results are shown to determine the efficiency of the proposed algorithm of DSTATCOM.

Key words: Current Control Mode, Voltage Source Inverter, Power Quality (PQ), Voltage-Control Mode

I. INTRODUCTION

The main problem associated with the present Distribution power system is the power quality issues like current and voltage distortion, and poor power factor. A DSTATCOM that is connected at the location of common coupling (PCC), is used for mitigating both types of Power Quality issues. During current control mode (CCM) of operation, it will injects harmonic components and reactive power of load currents so that source currents become sinusoidal, balanced, and in phase with the PCC voltages. During voltage-control mode of operation the DSTATCOM adjusts PCC voltage to a reference value to protect critical loads during voltage disturbances, such as swell, unbalances and sag. One Active filter is not enough to achieve the advantages of CCM and VCM as the two modes are independent of each other.

The main disadvantage of DSTATCOM in CCM is it cannot compensate for voltage disturbances. Hence it cannot be used for voltage disturbances. Normally, in Voltage control mode, the DSTATCOM maintains the PCC voltage at 1.0p.u. But the load works satisfactorily for a permissible voltage range only. To compensate the voltage drop in the feeder, DSTATCOM supplies an additional reactive current. This increases the total source currents, which increases additional losses in the feeder and Voltage-source inverter (VSI) and also require to have a higher current rating VSI. Capacity to mitigate deep voltage sag also decreases.

In this paper we consider the operation of DSTATCOM in VCM and a control algorithm is proposed to obtain the reference load terminal voltage. This algorithm will provide the combined advantages of CCM and VCM. By using this algorithm UPF Operation at the PCC is accomplished at nominal load, the required reactive component and harmonic component of load current is provided at any time by compensator. The deadbeat predictive controller is utilized to produce switching pulses. The control strategy is tested with a three-phase four-wire distribution system. The efficacy of the proposed algorithm is confirmed through the comprehensive simulation results. This paper is organized as follows: Chapter-2 discuss about the proposed control strategy. Chapter-3 presents the simulation results. In Chapter-4 conclusion is drawn from the above discussion.

II. PROPOSED CONTROL STRATEGY

In this paper we consider a three phase four wire two-level neutrally clamped Voltage Source Inverter is used. Figure 1 shows the circuit diagram of DSTATCOM compensated distribution system. Here independent control is given to each leg of the VSI. The equivalent circuit of Figure 1 is shown in Figure2.

Variable u is used as a switching function whose value is either +1 or -1 depending upon the switching state. The circuit consists of Filter inductance Lf and resistance Rf. Shunt capacitor Cf which eliminates the high-switching frequency components. By properly choosing these parameters of VSI we can control the PCC voltage at any required value.

A reference voltage magnitude derivation scheme is proposed that gives the benefits of CCM at nominal load. The overall controller block diagram is shown in Fig. 3.
A. Modeling Of System and Derivation of the Voltage-Control Law:

The circuit in Fig.2, state-space equations are given by

\[ \dot{x} = Ax + Bz \]  

(1)

Where

\[ A = \begin{bmatrix} 0 & - \frac{L_f}{C_f} & 0 \\ \frac{L_f}{C_f} & 0 & - \frac{1}{R_f} \\ 0 & 0 & 0 \end{bmatrix}, \quad B = \begin{bmatrix} 0 \\ \frac{1}{C_f} \\ 0 \end{bmatrix} \]

The general time-domain solution of (1) to compute the state vector \( x(t) \) with known initial value \( x(t_0) \), is given as follows:

\[ x(t) = e^{A(t-t_0)} x(t_0) + \int_{t_0}^{t} e^{A(t-\tau)} B z(\tau) d\tau. \]  

(2)

The equivalent discrete solution of the continuous state is obtained by replacing \( t_0 = kT_d \) and \( \tau = (k+1)T_d \) as follows:

\[ x(k+1) = e^{AT_d} x(k) + \int_{kT_d}^{(k+1)T_d} e^{A(T_d+\tau)} B z(\tau) d\tau. \]  

(3)

In (3), \( k \) and \( T_d \) represent the \( k \)th sample and sampling period, respectively. During the consecutive sampling period, the value of \( x(t) \) is held constant, and can be taken as \( x(k) \). After simplification and changing the integration variable, (3) is written as

\[ x(k+1) = e^{AT_d} x(k) + \int_{0}^{T_d} e^{A\tau} B d\lambda z(k). \]  

(4)

Equation (4) is rewritten as follows:

\[ x(k+1) = Gx(k) + Hz(k) \]  

(5)

where \( G \) and \( H \) are sampled matrices, with a sampling time of \( T_d \). For small sampling time, matrices \( G \) and \( H \) are calculated as follows:

\[ G = \begin{bmatrix} G_{11} & G_{12} & G_{13} \\ G_{21} & G_{22} & G_{23} \\ G_{31} & G_{32} & G_{33} \end{bmatrix} = e^{AT_d} \approx I + AT_d + \frac{A^2T_d^2}{2} \]  

(6)

\[ H = \begin{bmatrix} H_{11} & H_{12} & H_{13} \\ H_{21} & H_{22} & H_{23} \\ H_{31} & H_{32} & H_{33} \end{bmatrix} = \int_{0}^{T_d} e^{A\lambda} B d\lambda \]  

(7)

The capacitor voltage using (5) is given as

\[ v_{fc}(k+1) = G_{11}v_{fc}(k) + G_{12}i_{f1}(k) + H_{11}u(k) + H_{12}i_{f1}(k). \]  

(8)

As seen from (8), the VSI parameters \( C_f, V_{dc}, R_f, V_{dc} \) and sampling time \( T_d \) decides the reference terminal voltage. Hence VSI parameters require to be chosen with care. Let \( v^r_{f\tau} \) be the reference load terminal voltage. A cost function is chosen as follows

\[ J = \left( v_{fc}(k+1) - v^r_{f}(k+1) \right)^2. \]  

(9)

Differentiate cost function \( J \) with respect to \( u(k) \) and its minimum is

\[ u^*(k) = \frac{v^r_{f}(k+1) - G_{11}v_{fc}(k) - G_{12}i_{f1}(k) - H_{11}u(k) - H_{12}i_{f1}(k)}{H_{11}}. \]  

(10)

In (11), \( v^r_{f}(k+1) \) is the future reference voltage that is not known. Using Lagrange extrapolation method, prediction of this reference voltage is done as follows:

\[ v^r_{f}(k+1) = 3v^r_{f}(k) - 3v^r_{f}(k-1) + v^r_{f}(k-2). \]  

(12)

B. Design of VSI Parameters:

DSTATCOM regulates terminal voltage satisfactorily, by properly selecting the VSI parameters. The method of selection of these parameters is given as follows.

1) DC Bus Voltage (VDC):

The voltage across dc bus is taken double of the phase source voltage’s peak, for satisfactory performance. Hence, for a line voltage of 400 V, the dc bus voltage is kept at 650 V.

2) DC Capacitance:

Values of dc capacitors are chosen according to period of sag or swell and variations in dc bus voltage at the time of transients. Let the total load rating be kVA. In the worst case, the load power may vary from minimum to maximum that is, from 0 to 5 kVA.

3) Filter Inductance (Lf):

Inductance of filter is chosen such that reasonably high switching frequency and adequate rate of change of current.

C. Controller for DC Bus Capacitor Voltage

Average real power balance at the PCC will be
\[ P_{\text{pcc}} = P_{\text{load}} + P_{\text{loss}} \]

Where \( P_{\text{pcc}}, P_{\text{load}} \) and \( P_{\text{loss}} \) are the average PCC power, load power, and losses in the VSI, respectively. The power available at the PCC, which is taken from the source, depends upon the angle between source and PCC voltages, that is, load angle. Hence, must be maintained constant to keep constant.

The dc bus voltage of DSTATCOM can be regulated at its reference voltage by obtaining inverter losses \( P_{\text{loss}} \) from the source. \( P_{\text{loss}} \) can be made constant by maintaining capacitor voltage at a constant value. As a result \( \delta \) also becomes constant. Hence it is clear that dc link voltage can be maintained at reference value with development of suitable value of \( \delta \). This \( \delta \) incorporates the impact of losses from the VSI. To calculate load angle \( \delta \), the average of dc voltages \( V_{\text{dc1}} \) and \( V_{\text{dc2}} \) is matched with a reference voltage, and the difference is sent to a PI controller.

III. SIMULATION RESULTS

The control scheme is implemented using PSCAD software. Simulation parameters are given in Table I. Terminal voltages and source currents before compensation are plotted in Fig. 4. Distorted and unbalanced source currents flowing through the feeder make terminal voltages unbalanced and distorted. Three conditions, namely, nominal operation, operation during sag, and operation during load change are compared between the traditional and proposed method. In the traditional method, the reference voltage is 1.0 p.u.

![Fig. 4: Without Compensation. (A) Terminal Voltages. (B) Source Currents](image)

<table>
<thead>
<tr>
<th>System parameters</th>
<th>Values</th>
</tr>
</thead>
<tbody>
<tr>
<td>Voltage of source</td>
<td>400V RMS line to line 50Hz</td>
</tr>
<tr>
<td>Impedance of feeder</td>
<td>( Z_s = 1 + j3.1428 \Omega )</td>
</tr>
</tbody>
</table>
| Linear Load | \( Z_{la} = 30 + j62.857 \Omega \)  
| | \( Z_{lb} = 40 + j78.57 \Omega \)  
| | \( Z_{lc} = 50 + j50.285 \Omega \) |

Table 1: Simulation Parameters

A. Nominal Operation:

Initially, the traditional method is considered. Figure 5(a)–(c) shows the regulated terminal voltage & corresponding source currents in phases a, b, and c respectively. These waveforms are balanced and sinusoidal. However, source currents lead respective terminal voltages which show that the compensator supplies reactive current to the source to overcome feeder drop, in addition to supplying load reactive and harmonic currents.

![Fig. 5: Terminal Voltages And Source Currents Using The Traditional Method. (A) Phase-A. (B) Phase-B. (C) Phase-C](image)

Fig. 6(a) shows the voltage of dc bus maintained at a nominal voltage of 1300V. Fig. 6(b) shows the load angle steady around 8.50°.
Using the proposed method, voltages at terminal and currents of source in phases a, phase b, and phase c are shown in Fig. 7(a) to Fig. 7(c), respectively. It can be observed that the corresponding terminal voltages and source currents are in phase with each other, along with that they are balanced and sinusoidal. Hence, UPF is obtained at the load terminal.

B. Operation during Sag:

To generate sag, voltage of source is reduced by 20% of its nominal value at 0.6 s as shown in Fig. 8(a). Without sag i.e. 1.0 s as shown in Fig. 8(b). Fig. 8(c) and (d) shows voltages at terminals maintained at their reference value.

The controller delivers a fast regulation of voltage at the load terminal. Fig. 8(e) and Fig. 8(f) shows the total voltage of dc bus and the load angle, respectively. For the period of transient, capacitors discharges in order to maintain load power, which makes to get more power from the source as compared to normal operation.
C. Operation during Load Change:

To show the impact of load changes on system performance, load is increased to 140% of its nominal value. Under this condition, the traditional method gives less power factor as the compensator will supply more reactive current to maintain the reference voltage. The voltage and current waveforms, as shown in Fig. 9(a), confirm this. In proposed method, a load change will result in small deviation in terminal voltage from its reference voltage. Compensator just needs to supply extra reactive current to overcome this small extra feeder drop, hence, nearly UPF is obtained while maintaining the terminal voltage at its reference voltage. It is evident from Fig. 9(b).

IV. CONCLUSION

The performance of the proposed scheme is compared with the traditional voltage-controlled DSTATCOM. The proposed method provides the following advantages: 1) at nominal load, the compensator infuses harmonic component and reactive component of load current, resulting in UPF; 2) nearly UPF is maintained for a load change; 3) fast voltage regulation has been achieved during voltage disturbances; and 4) losses in the VSI and feeder are reduced considerably, and have higher sag supporting capability with the same VSI rating compared to the traditional scheme.

REFERENCES


