A Review on Low Power Design and Verification Techniques

Bua Baker

1Department of Electronics and Communication Engineering
1Gujarat Technological University PG School, Gujarat Technological University, Ahmedabad – 382 424, Gujarat - India

Abstract— In this paper, the fundamental components of low power design and verification are explained in addition to how the UPF (Unified Power Format) with modern techniques facilitates the Power-Aware verification at the RTL, with conventional RTL (Register Transfer Level) design techniques plus reusable blocks.

Key words: Low Power, Verification, Unified Power Format, Register Transfer Level, Power-Aware

I. INTRODUCTION

As the complexity in power architecture as well as complex power domain partitioning increases, it becomes essential to make functional as well as physical verification of this complex power logic concurrently [1]. Conversely, regardless of persistent endeavours of verification engineers, a few problems can still escape making their way through to silicon. In order to evade silicon malfunctions due to low power concerns, engineers have to discover modern methodologies to deal with unpredicted low power concerns [1]. The need for Low Power Design is driven by the growing consumer demand for portable electronics such as Cell Phones, Smart Phones, Tablets, Laptops, etc.

The high-tech performance, battery-operated and SoC (System-on-Chips) in communication and computing is changing the centre of attention from conventional limitations (for instance area, performance, cost and reliability) to power consumption [3].

Every new generation is anticipated to comprise of extra features as well as longer battery life. Also another driving demand for Low Power Design is the initiative of governments and industries to decrease worldwide energy consumption [3].

II. LOW POWER DESIGN

The Low Power Design requires active power management which is becoming more important at 90nm and necessary below 65nm. Active power management involves the application and control of power reduction techniques to decrease power consumption, in particular static leakage [2].

Power consumption at process nodes less than 100 nm owing to static energy loss or leakage is being linked to switching activity or dynamic power consumption as the main power management concern. It is being detailed that leakage represents above 40 percent of overall power expenses at the 65 nm technology node [2].

The rising cost of leakage is in relation to the fact that with a smaller geometry, the silicon partition becomes thinner, hence greater the energy drain owing to leakage.

Conventional low power design techniques, for instance, decreasing the power supply voltage (VDD) as well as clock gating become less efficient and can become detrimental as voltage decrease adds to circuit delay [2].

To sustain performance, designers balance this improved delay by reducing the threshold voltage. Adversely, this drastically raises leakage current because of the exponential characteristics of leakage current within the transistor sub-threshold system [2].

III. POWER IMPACTS ON SYSTEM DESIGN

1) Energy consumed per task establishes battery life i.e. the second order effect is that higher current draws decrease efficient battery energy capacity [7].

2) Current draw results into IR drops in power supply voltage thus requiring extra power/ground pins to decrease resistance R and thick as well as wide on-chip metal wires or else dedicated metal layers [7].

3) Switching current (dI/dT) results into inductive power supply voltage bounce = LdI/dT which in turn needs more pins/shorter pins to decrease inductance L. Also needs on-chip/on-package decoupling capacitance to aid bypass pins all through switching transients [7].

4) Power dissipated as heat results into higher temperatures which reduces speed and reliability thus need for further expensive packaging as well as cooling systems [7].

IV. POWER REDUCTION TECHNIQUES

These include [7];

A. Clock Gating:

To turn off the clock to avoid unnecessary switching activity when logic blocks are not in use.
B. Power Gating:
To shut off power itself when logic is not in use thus avoiding power loss due to static leakage of that block.

![Power Gating Architecture](image)

C. Multi-Voltage Design:
To optimize power used for required performance.

![Architecture for Multi-Voltage Design](image)

D. Voltage/Frequency Scaling:
To dynamically adjust power, that is voltage and frequency, for required performance.

![Voltage/Frequency Scaling Architecture](image)

V. POWER MANAGEMENT CONCEPTS
Many techniques over the years are being developed to deal with the constantly destructive power reduction conditions of nearly all ASIC and SoC designs [2]. These techniques employ several type of sleep mode operation since power management techniques utilize switching on and off different sections of a design which are partitioned into different power domains basing on areas of functionality supporting familiar operations or else tasks [2].

A. Power Domains:
These are independently powered regions that enable application of different power reduction techniques in each region. Additionally, each power aware design as a minimum has a single primary domain that is all the time on and it is known as the wake-up or always-on domain.

B. State Retention/Retention Memory Elements:
Applied to save essential data when power is off and to enable quick resumption after power up i.e. retaining the state of registers as well as latches in sleep mode. UPF supports the specification of retention as well as isolation strategies on the implementation of low power design functions.

C. Isolation Cells:
When power domain driving a net is power down and domain receiving a net is powered up then isolation is required between domains to ensure correct electrical and logical interactions between domains in different power states.

D. Level Shifting:
When two domains are operated at different voltage levels then signal sent from one to the other must be level shifted to ensure correct communication between domains operating at different voltage levels. UPF supports the specification of level shifter strategies together with voltage tolerance threshold to check if the strategy affects the up-shift, down-shift, or both.

E. System Power States and the Supply Network:
The UPF permits specification of the entire supply network information required for verification and implementation of the power supply distribution which offers the control needed to understand the system power states. UPF also automates the links of the supply network with logic elements in the design supported by the semantics classified for specific supply nets types.

VI. POWER MANAGEMENT DESIGN STRUCTURE/ARCHITECTURE
It utilizes the following concepts to apply power reduction techniques to design [2]:

![Power Management Design Structure](image)
A. **Power Domain Partitioning:**
Defines independent power managed regions.

B. **Power Domain Interactions:**
Isolation and/or level shifting logic inserted at power domain boundaries.
State Initialization/Restoration: Reset logic and/or retention registers.

C. **Power Distribution:**
The power distribution supply network includes power switches, supply ports defining power domains and switches, supply nets for connecting supply ports, logic ports and propagating the supply state and the supply states. Every supply port has either one or extra supply states classified.

D. **Power States:**
Of supplies, domains, sub-systems and system. In the design of low power features of an electronic system, one must begin with the system power states definition

E. **Power Control Logic:**
Centralized or distributed hardware and/or software.

**VII. NORMAL DESIGN AND VERIFICATION FLOW**

A. **RTL design:**
This captures design intent, drives functional verification and synthesis.

B. **Logical Implementation:**
Using standard cells, macros and further modified for test, ECOs, etc.

C. **Physical Implementation:**
Where Place and Route completes the implementation and produces manufacturing data.

D. **Power Management:**
Is the inherently part of physical implementation which should be considered in earlier stages.

**VIII. LOW POWER DESIGN AND VERIFICATION FLOW WITH UPF**
The specifications of low power are required at every step during design flow in order that the right power management elements may be employed at the RTL, deduced properly through synthesis as well as placed-and-routed proficiently and correctly during physical design [5]. One power format simplifies implementation in addition to validation and facilitates meeting design plans while addressing reusability, permitting early and systematic validation as well as include built-in extensibility [5].

**Fig. 7: Normal Design and Verification Flow**

A. **RTL Is Augmented With UPF:**
So as to define the power architecture for a given implementation.

B. **RTL and UPF Verification:**
This ensures that the power architecture is complete and consistent with expected power states of the design. That is, to make sure the design will work correctly under power management with this power architecture.

C. **RTL and UPF Implementation:**
It involves Synthesis, test insertion, place and route, etc. UPF can be updated by the user or the tool.

D. **Netlist And UPF Verification:**
This includes Power aware equivalence checking, static analysis, simulation, emulation, etc. With application of reliable semantics designed for verification as well as implementation, UPF maintains a multi-tool flow of verification to facilitate simulation along with equivalence checking tools to completely validate the low power design intent from RTL to GDSII.

**IX. THE SIMULATION FLOW FOR POWER AWARE**
The functional verification problem of power aware designs is solved by power aware simulation (PA Simulation) which provides designers the capability of functionally verifying their power management techniques at the RTL decreasing costs considerably in regard to effort and time [4].
Fig. 9: Simulation flow with Power Aware Modelling using Questa.

Four broad categories of PA Simulation [4]:

A. Register/Latch Recognition from the RTL Design:
Register, latch and memory recognition from the HDL in general is related to the front-end of synthesis that converts the HDL into the structural netlist which consists of flip-flops, latches, memories as well as combinatorial logic.

B. Identification of Power Elements and Their Power Control Signals:
The simulator is capable of creating the PCN by using the UPF and sequential element information, superimposing the functional network through the PCN as well as integrating the specified power-aware behaviour along with the RTL functionality.

C. Elaborating the Power Aware Design:
Power management can be of software or hardware control, which drives the signals defining the PCN based on the system’s power management strategy such as signaling power domains to retain state, enable isolation, power down, power up, disable isolation as well as restore state. In elaboration, the tool automatically routes the PCN according to the power specification in the UPF. Simulation verifies if the working of the system is correctly when the low power design intent is implemented as specified.

D. Power Aware Simulation:
The PA simulation begins normally once integration of the low power design specification with the RTL functional specification is done. Usually, the testbench, imitating the SW power management system implements the PMB through different system power states by switching power supplies, enabling or disabling isolation, gating clocks as well as executing save along with restore protocols.

X. CONCLUSION
The modern low power design specification with UPF standardization allows engineers portability to describe power distribution structural designs, power aware strategy creation as well as verification of their low power designs during the RTL to GDSII flow.

XI. ACKNOWLEDGMENT
My most heartfelt gratitude goes to the management and staff of Gujarat Technological University PG School Ahmedabad for giving me the opportunity to use the resources, expert advice and encouragement to come up with this work successfully.

REFERENCES