

Design and Implementation of Diode Clamped Multilevel Inverter using Matlab Simulink

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Abstract— This project presents the diode-clamped inverter (neutral-point clamped) topology. The project also presents the most relevant control and modulation method developed for this family of converters: multilevel sinusoidal pulse width modulation. Finally, the peripherally developing areas such as high-voltage high-power use Multilevel Inverters for future development are addressed. Furthermore, in this study, reduction of harmonics has been stressed on using Diode Clamped Multilevel Inverters (DCMLI). It also states the adverse effects of Total Harmonic Distortion (THD) on generation and transmission equipments. It also explains about Common Mode Voltage and its effects in brief. Multilevel Inverters have been designed, modeled and simulated and the output results have been depicted in the form of waveforms, THD analysis modules using MATLAB SIMULINK and the results are systematically tabulated. The percentage of THD is reduced as the number of levels is increased.

Key words: Adjustable Speed Drives, Multilevel Inverters, PWM, THD, DCMI

I. INTRODUCTION

Harmonic voltages and currents in an electric power system are due to the result of non-linear electric loads. In power grid harmonic frequencies are a frequent cause of power quality problems. Harmonics in power system result in high increase of heating in the equipment and conductors, torque pulsations in motors, and misfiring in variable speed drives etc.

A. Current Harmonics

In a power system normal alternating current varies sinusoidal at a specific frequency, usually 50 or 60 hertz. When a linear electrical load is connected to the system, it draws a sinusoidal current at same frequency as the voltage (though usually not in phase with the voltage).

Current harmonics are caused by non-linear loads. When a non-linear load, such as a rectifier, is connected to the system, it draws a current that is not necessarily sinusoidal. The current waveform can become quite complex, depending on the type of load and its interaction with other components of the system. Regardless of how complex the current waveform becomes, as described through Fourier series analysis, it is possible to decompose it into a series of simple sinusoids, which start at the power system fundamental frequency and occur at integer multiples of the fundamental frequency.

Further examples of non-linear loads include common office equipment such as computers and printers, Fluorescent lighting, battery chargers and also variable-speed drives.

B. Voltage harmonics:

Voltage harmonics are mostly caused by current harmonics. The voltage provided by the voltage source will be distorted by current harmonics due to source impedance. If the source impedance of the voltage source is small, current harmonics will cause only small voltage harmonics.

C. Total Harmonic Distortion

Total harmonic distortion, or THD is a common measurement of the level of harmonic distortion present in power systems. THD is defined as the ratio of total harmonics to the value at fundamental frequency.

$$THD = \frac{\sqrt{V_2^2 + V_3^2 + V_4^2 + \dots + V_n^2}}{V_1}$$

where V_n is the RMS voltage of n th harmonic and $n = 1$ is the fundamental frequency.[1]

D. Effects

One of the major effects of power system harmonics is to increase the current in the system. This is particularly the case for the third harmonic, which causes a sharp increase in the zero sequence current, and therefore increases the current in the neutral conductor. This effect can require special consideration in the design of an electric system to serve non-linear loads. In addition to the increased line current, different pieces of electrical equipment can suffer effects from harmonics on the power system.

II. MULTILEVEL INVERTER

Multilevel inverter is based on the fact that sine wave can be approximated to a stepped waveform having large number of steps. The steps being supplied from different DC levels supported by series connected batteries or capacitors. The unique structure of multi-level inverter allows them to reach high voltages and therefore lower voltage rating device can be used. As the number of levels increases, the synthesized output waveform has more steps, producing a very fine stair case wave and approaching very closely to the desired sine wave. It can be easily understood that as motor steps are included in the waveform the harmonic distortion of the output wave decrease, approaching zero as the number of levels approaches infinity. Hence Multi-level inverters offer a better choice at the high power end because the high volt-ampere ratings are possible with these inverters without the problems of high dv/dt and the other associated ones.

The basic three types of multilevel topologies used are:

- 1) Diode clamped multilevel inverters
- 2) Flying capacitors multilevel inverter or Capacitor clamped multilevel inverter
- 3) Cascaded inverter with separate dc source.

A. Diode-Clamped Multilevel Inverter

The diode-clamped type inverter is used for experimentations in this project. Such inverter employs the technique of proportional stepping harmonic elimination type to control switching equipment in the circuit for providing appropriated waveform and increasing the efficiency at high loading. The diode-clamp and modulate principle are implemented to control the output waveform approaching to the sine-wave as close as possible.

The most commonly used multilevel topology is the diode clamped inverter, in which the diode is used as the clamping device to clamp the dc bus voltage so as to achieve steps in the output voltage. Thus, the main concept of this

inverter is to use diodes to limit the power devices voltage stress. The voltage over each capacitor and each switch is V_{dc} . An m level inverter needs $(m-1)$ voltage sources, $2(m-1)$ switching devices and $2(m-2)$ diodes. By increasing the number of voltage levels the quality of the output voltage is improved and the voltage waveform becomes closer to sinusoidal waveform.

III. MODELING OF INVERTERS

A. Two Level Inverter

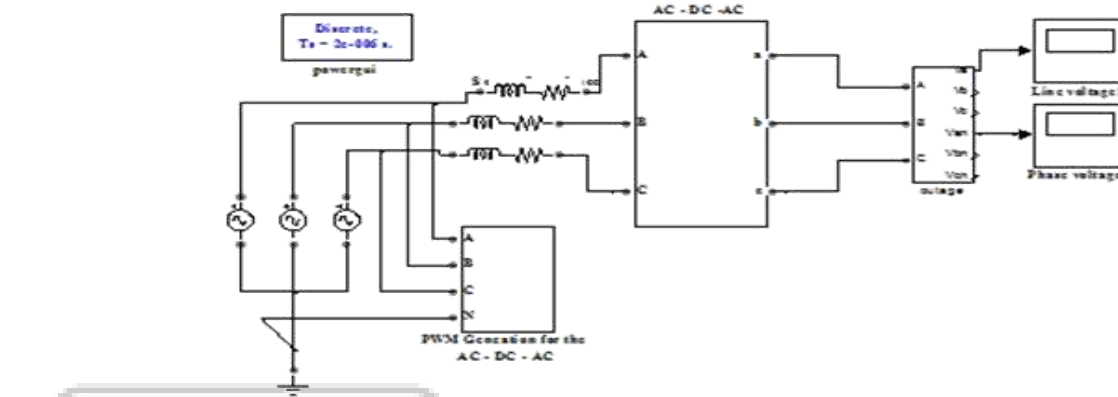


Fig. 1: Two level inverter simulink model

1) PWM Signal Generation

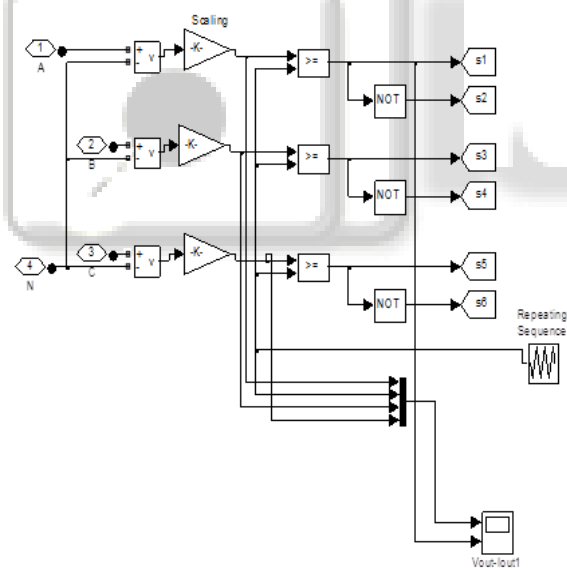


Fig. 2: PWM signal generation

To explain how the staircase voltage is synthesized, the neutral point n is considered as the output phase voltage reference point. There are two switch combinations to synthesize two-level voltages across a and n .

- Voltage level $V_{an} = V_{dc}/2$, turn on the switch $Sw1$.
- Voltage level $V_{an} = 0$, turn off the switches.
- Voltage level $V_{an} = -V_{dc}/2$ turn on the switch $Sw1'$.

2) Line And Phase Voltage Thd Analysis

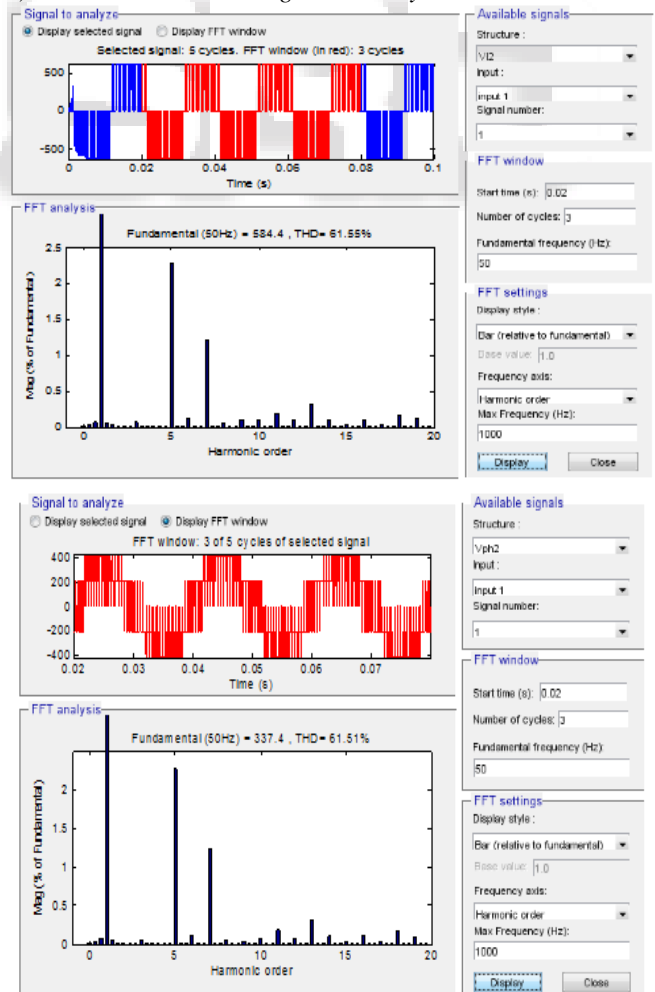


Fig. 3: Line and Phase Voltage THD Analysis

B. Three Level Inverter

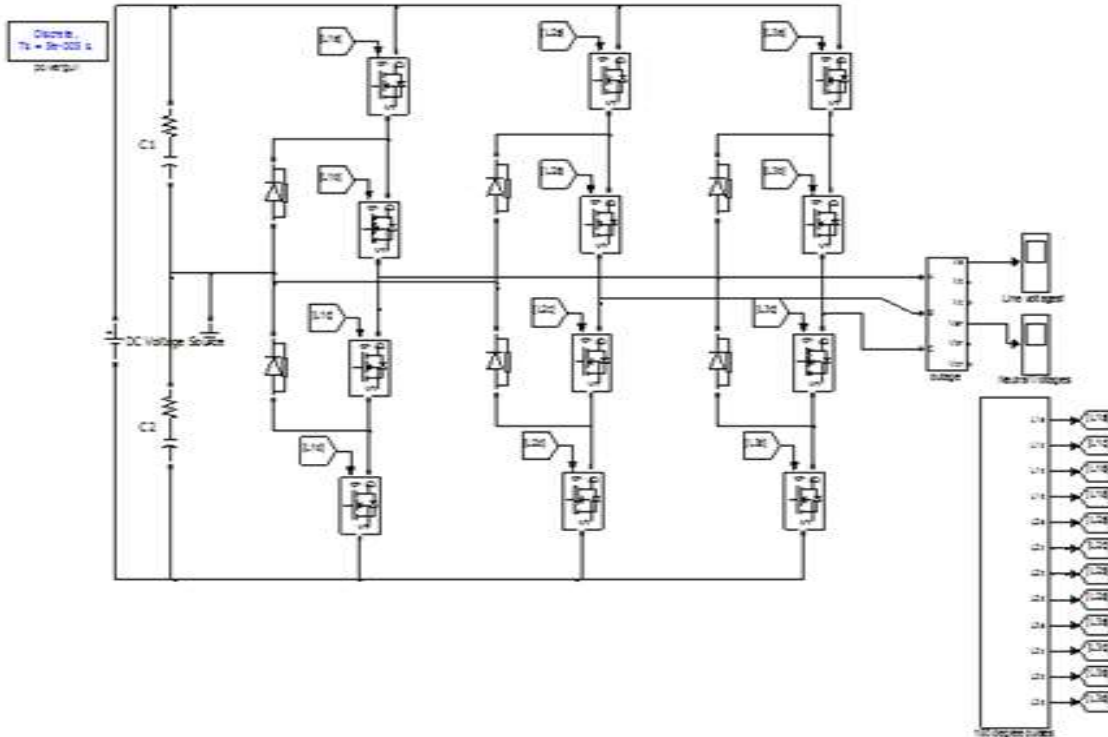


Fig. 4: Three level inverter simulink model

Figure shows a three-level diode-clamped converter in which the dc bus consists of two capacitors, C1, C2.

For dc bus voltage V_{dc} , the voltage across each capacitor is $V_{dc}/2$ and each device voltage stress will be limited to one capacitor voltage level $V_{dc}/2$ through clamping diodes.

To explain how the staircase voltage is synthesized, the neutral point n is considered as the output phase voltage

reference point. There are three switch combinations to synthesize three-level voltages across a and n.

- Voltage level $V_{an} = V_{dc}/2$, turn on the switches Sw1 and Sw2.
- Voltage level $V_{an} = 0$, turn on the switches Sw2 and Sw1'.
- Voltage level $V_{an} = -V_{dc}/2$ turn on the switches Sw1', Sw2'.

1) PWM Signal Generation

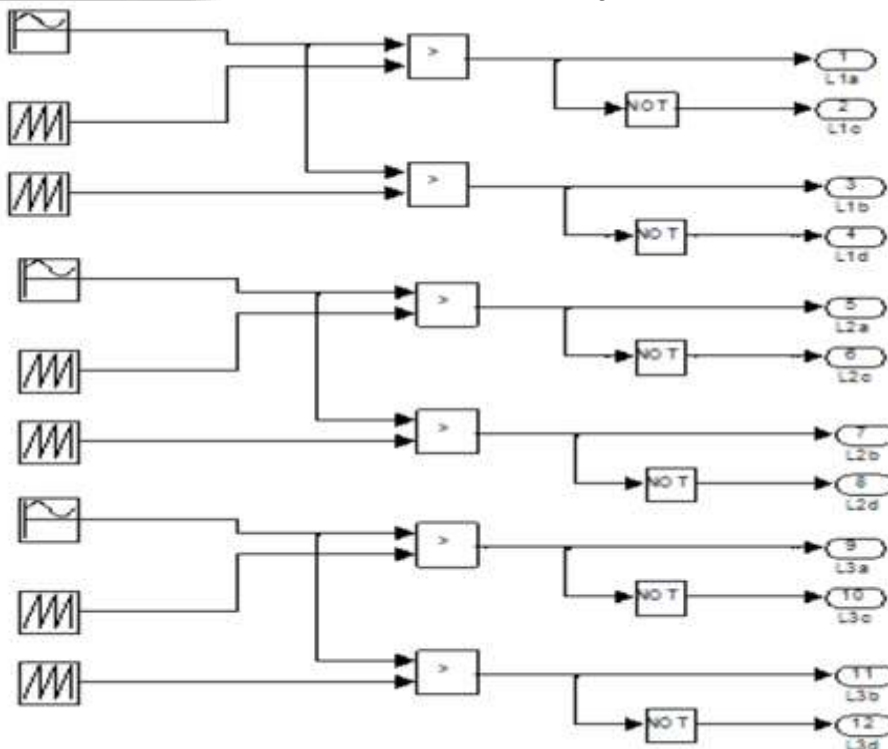


Fig. 5: PWM signal generation

2) Line And Phase Voltage THD Analysis

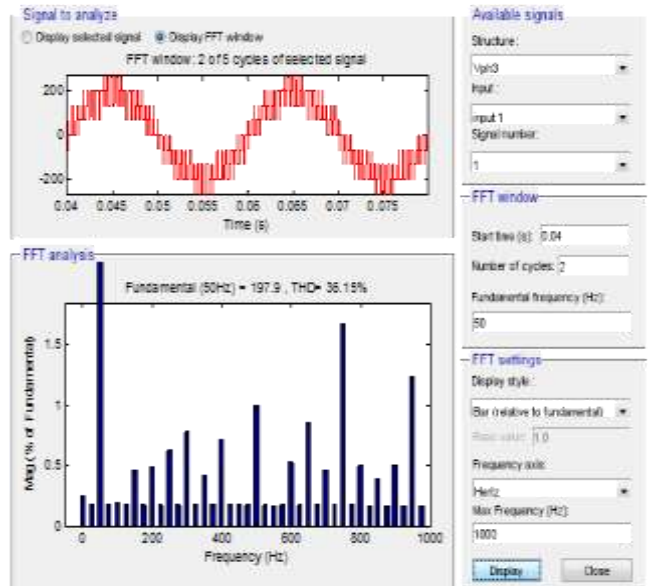
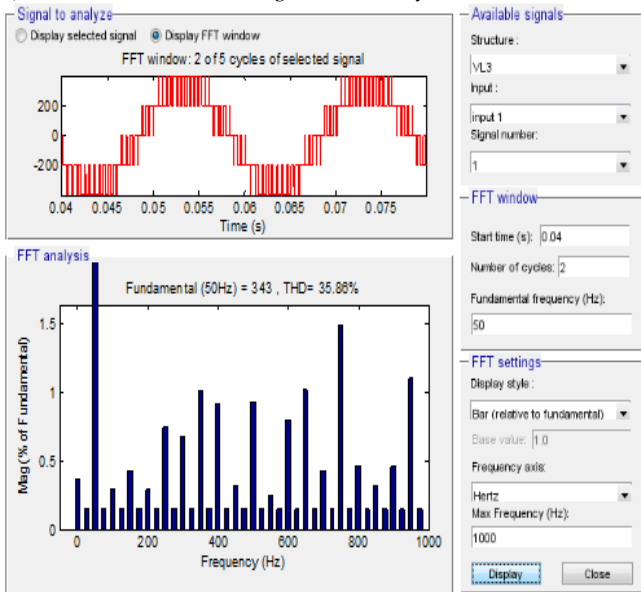


Fig. 6: Line and Phase Voltage THD analysis

C. Five Level Inverter

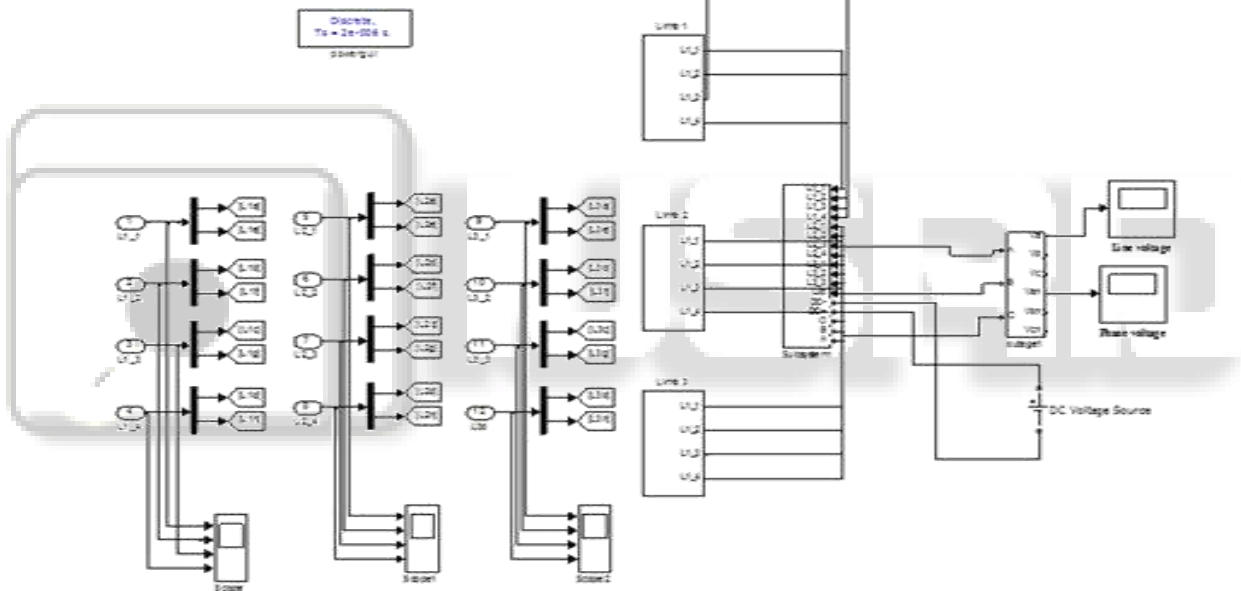
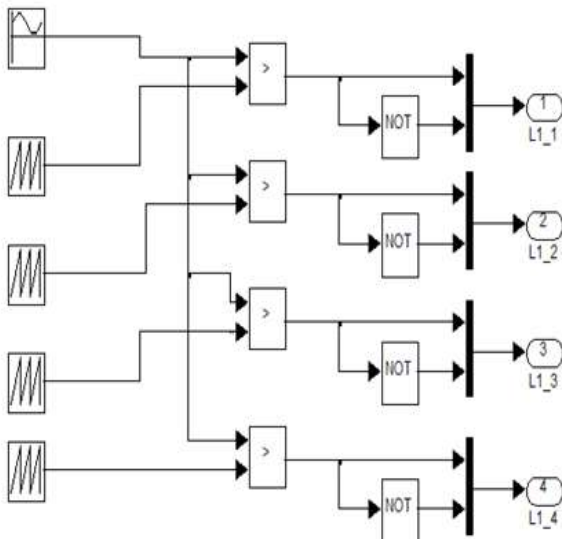


Fig. 7: Five level simulation model

1) PWM Signal Generation



2) Five Level Diode Clamped Circuit

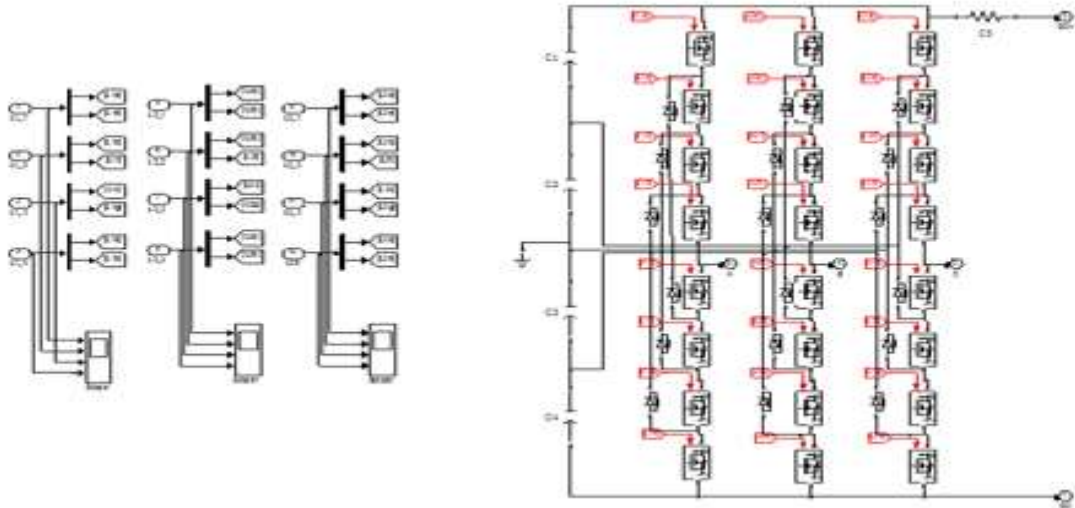


Fig. 8: Five level inverter simulink model

Figure shows a five-level diode-clamped converter in which the dc bus consists of four capacitors, C1, C2, C3, and C4. For dc-bus voltage V_{dc} , the voltage across each capacitor is $V_{dc}/4$ and each device voltage stress will be limited to one capacitor voltage level $V_{dc}/4$ through clamping diodes.

The order of numbering of the switches for phase a is Sw1, Sw2, Sw3, Sw4, Sw1', Sw2', Sw3' and Sw4'.

For example to have $V_{dc}/2$ in the output, switches Sw1 to Sw4 should conduct at the same time. For each voltage level four switches should conduct.

The steps to synthesis the five level phase a output voltage in this work are as follows:

- For phase a output voltage of $V_{an}=0$, two upper switches Sw3, Sw4 and two lower switches Sw1' and Sw2' are turned on.
- For an output voltage of $V_{an}=V_{dc}/4$, three upper switches Sw2, Sw3, Sw4 and one lower switch Sw1' are turned on.
- For an output voltage of $V_{an}=V_{dc}/2$, all upper switches Sw1 through Sw4 are turned on.
- To obtain the output voltage of $V_{an}= -V_{dc}/4$, upper switch Sw4 and three lower switches Sw1', Sw2' and Sw3' are turned on.
- For an output voltage of $V_{an} = -V_{dc}/2$, all lower switches Sw1' through Sw4' are turned on.

3) Line And Phase Voltage THD Analysis

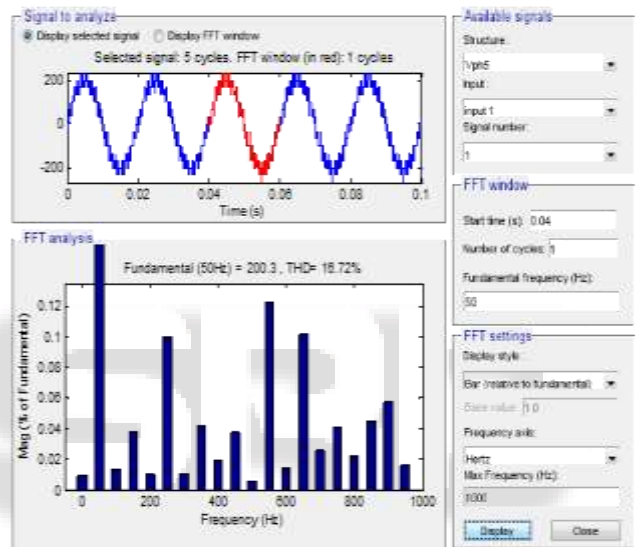
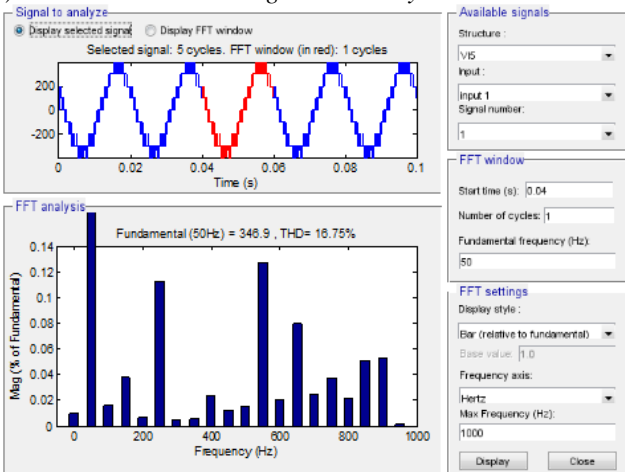


Fig. 9: Line and Phase voltage THD analysis

D. Seven Level Inverter

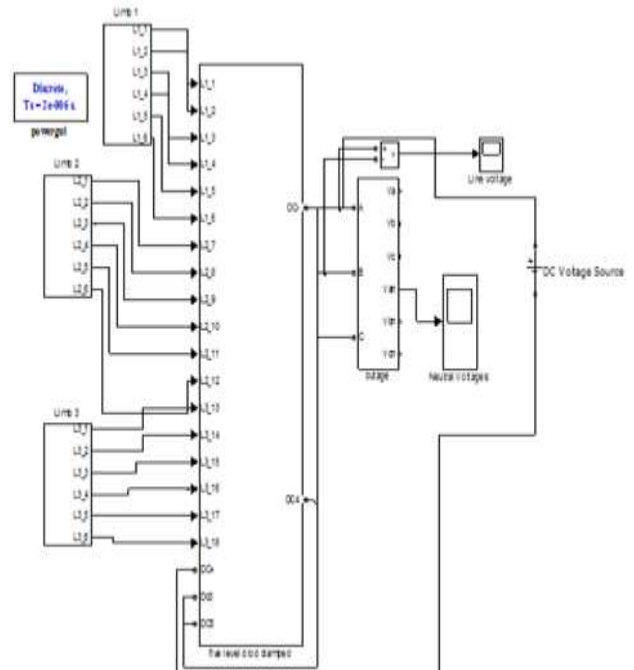


Fig. 10: Seven level inverter simulink model

1) PWM Signal Generation

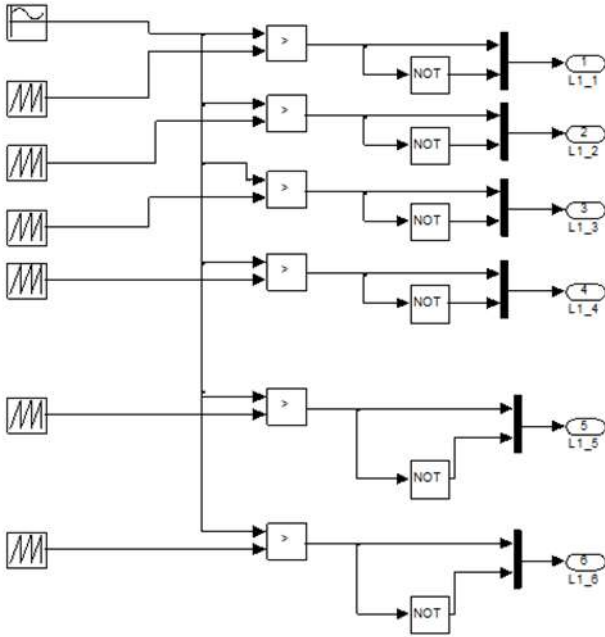


Fig. 11: PWM signal generation

2) Seven Level Diode Clamped Circuit

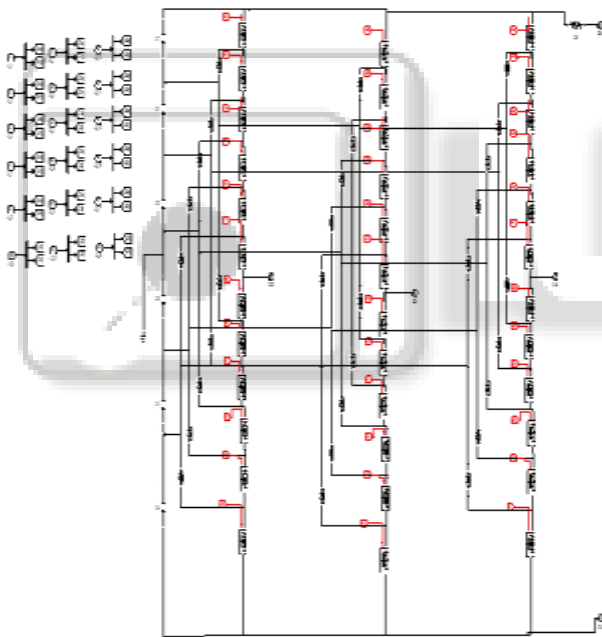


Fig. 12: Seven level inverter simulink model

- To produce a staircase-output voltage, consider one leg of the seven-level inverter. The steps to synthesize the seven-level voltages are as follows.
- For an output voltage level $V_{ao}=V_{dc}$, turn on all upper-half switches $Sw1, Sw2, Sw3, Sw4, Sw5$ and $Sw6$
- For an output voltage level $V_{ao}= 5V_{dc}/6$, turn on upper switch $Sw2, Sw3, Sw4, Sw5, Sw6$ and one lower switch $Sw1'$.
- For an output voltage level $V_{ao}= 4V_{dc}/6$, turn on upper half switches $Sw3, Sw4, Sw5, Sw6$ and lower switches $Sw1', Sw2'$.
- For an output voltage level $V_{ao}= V_{dc}/2$, turn on upper half switches, $Sw4, Sw5, Sw6$, and lower switches $Sw1', Sw2', Sw3'$.

- For an output voltage level $V_{ao}= V_{dc}/3$, turn on upper half switches, $Sw5, Sw6$, and lower switches $Sw1', Sw2', Sw3', Sw4'$.
- For an output voltage level $V_{ao}= V_{dc}/6$, turn on upper half switches, $Sw6$ and lower switches $Sw1', Sw2', Sw3', Sw4', Sw5'$.
- For an output voltage level $V_{ao}= 0$, turn on all lower half switches, $Sw1', Sw2', Sw3', Sw4', Sw5'$ and $Sw6'$.

3) Line and Phase Voltage THD Analysis

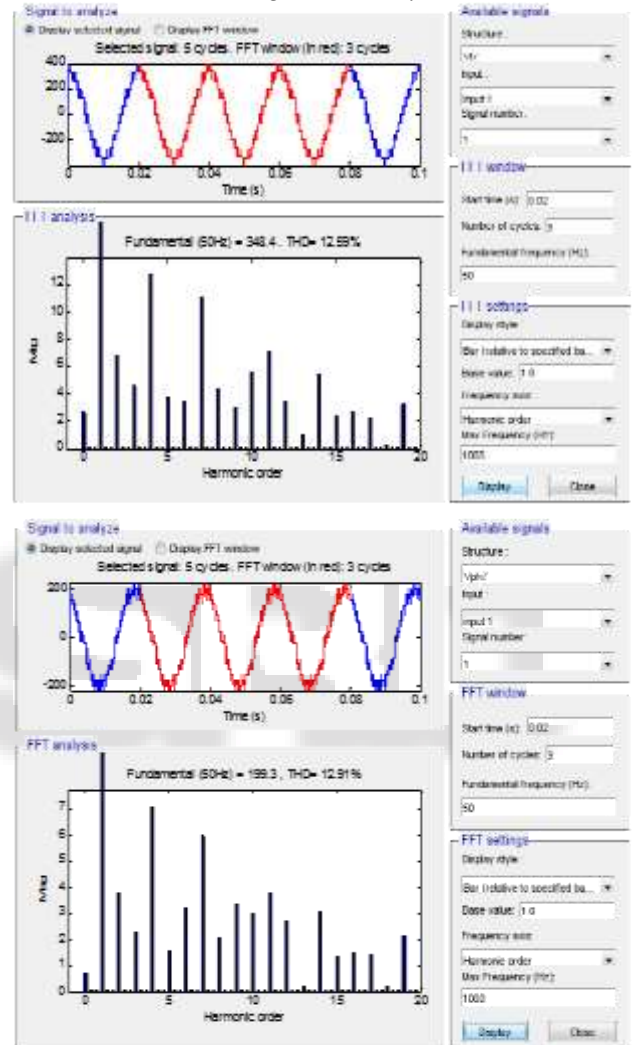


Fig. 13: Line and Phase voltage THD analysis

IV. RESULT

LEVEL	% of THD (in line)	% of THD (in phase)
2	61.55	61.51
3	35.86	36.15
5	16.75	16.72
7	12.59	12.91

Table 1: Comparison of line and phase voltage THD's for 2-level and multi-level inverters.

Fig. 14: Comparison of line and phase voltage THD's

V. CONCLUSION

This project has provided a brief summary of multilevel inverter circuits and their control. However, the commercial products that utilize this superior circuit topology were not available until the mid-1990s. Today, more and more commercial products are based on the multilevel inverter structure, and more and more worldwide research and development of multilevel inverter-related technologies is going on. This project cannot cover or reference all the related work, but the fundamental principle of different multilevel inverters has been introduced systematically.

The final THD(Total Harmonic Distortion) results as obtained from the designing, modeling and simulation of different levels of Multilevel Inverters has been represented using waveforms and THD(Total Harmonic Distortion) analysis and have been systematically in the final result table(TABLE 1).

REFERENCES

- [1] Akash A. Chandekar, R.K.Dhatrak, Dr.Z.J.Khan , Modelling and simulation of diode clamp multilevel inverter fed three phase induction motor for cmv analysis using filter, International.Journal.of Advanced Research in Electrical, Electronics and Instrumentation Engineering,(An ISO 3297: 2007 Certified Organization)Vol. 2, Issue 8, August 2013.
- [2] S.Shalini Assistant Professor, Department of Electrical and electronics engineering Roever Engineering College, Perambalur, Anna university, Tamilnadu, Voltage Balancing in Diode Clamped Multilevel Inverter Using Sinusoidal PWM International Journal of Engineering Trends and Technology (IJETT) – Volume 6 Number 2 - Dec 2013 ISSN: 2231-5381.
- [3] Varsha Sahu ,Shraddha Kaushik A New Five-Level Diode Clamp Multilevel Inverter Topology , International Journal Of Creative Research Thoughts,Volume 1, Issue.4, April 2013.
- [4] Mr.S.Ebanazar Pravin, Ms.R.Narciss Starbell, Induction Motor Drive Using Seven Level Multilevel Inverter for Energy Saving in Variable Torque Load Application, International Conference on Computer, Communication and Electrical Technology – ICCET 2011, 18th & 19th March, 2011.
- [5] Ehsan Najafi and Abdul Halim Mohamed Yatim, Design and Implementation of a New Multilevel Inverter Topology, IEEE. Transactions. On. Industrial. Electronic, VOL. 59, NO. 11, NOVEMBER 2012.
- [6] .JoseRodríguez, Senior Member, IEEE, Jih-Sheng Lai, Senior Member, IEEE, and Fang Zheng Peng, Senior Member, IEEE, Multilevel Inverters: A Survey of Topologies, Controls, and Applications, IEEE TRANSACTIONS ON Industrial Electronics, VOL. 49, NO. 4, AUGUST 2002.
- [7] Doron Shmilovitz, On the Definition of Total Harmonic Distortion and Its Effect on Measurement Interpretation, IEEE Transactions On Power Delivery, VOL. 20, NO. 1, JANUARY 2005.