Design of Low Power and High Speed Carry Select Adder

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Abstract— High Speed and lower power dissipation are trend in Digital Integrated circuit leads researcher to focus on modification in architecture level, topology level, system level, circuit level, and physical level design. Adder is a critical block for high speed and low power design of microprocessor, digital signal processor etc. Various architecture of adder has been proposed. Carry select adder (CSLA) is one of the high speed adder used in many data processing architectures. This paper pivots on diverse architecture of CSLA. Even grouping conventional CSLA and Binary-to-Excess-1 converter (BEC) CSLA have been implemented and compared with D-Latch CSLA.

Key words: Carry Select Adder (CSLA), Ripple Carry Adder (RCA), Full-adder (FA), Binary to Excess-1 (BEC) and D-Latch

I. INTRODUCTION

Low-power, area-efficient, and high-performance VLSI system are increasingly used in portable and mobile device, multi standard wireless receivers, and biomedical instrumentation [4]. Addition usually impacts widely the overall performance of digital systems like a multiplier, DSP to execute various algorithms like FFT, FIR and IIR[1]. The CSLA is used in many computational systems to alleviate the problem of carry propagation delay by independently generating multiple carries and then select a carry to generate the sum.

In the Carry select adder (CSLA) generally consists two Ripple Carry Adder and Multiplexer working with two input carry 1 and 0,and RCA Cin=1 block Modified into the Binary to Excess-1 (BEC) converter circuit to achieve lower area and power consumption with slightly increase in the delay. Further BEC block can be replaced by D-Latch to improve the performance.

The rest of this brief is organized as follows: Regular and Modified CSLA detail structure of BEC is presented in Section II and III. Explain about the Improved CSLA architecture is presented in Section IV. Comparisons of power and delay Comparison Result are analysis is presented in Section V. The conclusion is given in Section VI.

II. 16-BIT CSLA USING DUAL RCA

The basic conventional CSLA generally consists of two Ripple carry adder (RCA) and a Multiplexer (MUX). The main disadvantage of Regular CSLA is the large area due to the multiple Pairs of RCA. As shown in Fig.1, 16-bit Regular CSLA divided into five groups with different bit size of RCA. First two groups are two bit RCA and other groups are four bit RCA.

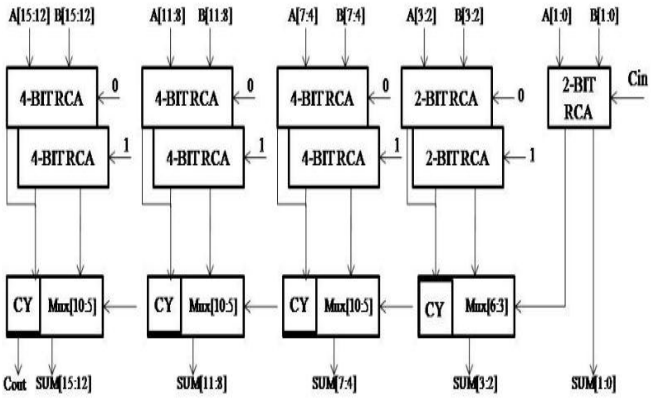

Fig.1: Architecture of 16-bit Regular CSLA

First block of conventional 16-bit CSLA contain 2-bit RCA with one input carry and generating two outputs: one 2-bit Sum and output carry, which used as selection line for next block multiplexer. Other block performs the calculation twice, one time with the assumption of the carry being zero and the other assuming one. After two results are calculated the correct sum, as well as the correct carry, is then selected with the multiplexer using pervious stage carry.

III. MODIFIED 16-BIT CSLA USING BEC

The Modified CSLA has a one RCA with Binary to Excess-1 converter. Here we use the Binary to Excess-1 Converter (BEC) instead of RCA with Cin=1 in the conventional CSLA .The Fig.2 shows the structure of 16-bit Modified CSLA divided into five groups with different bit size of RCA and BEC .To replace the N-bit RCA , an N+1-bit BEC is required. Modified CSLA 4-bit BEC block delay is 0.934ns and 4-bit RCA block delay is 8.959ns.

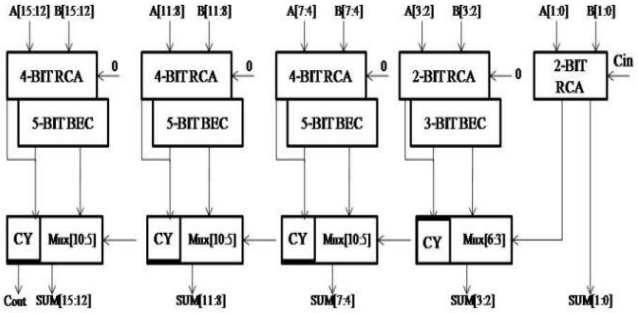

Fig.2: Architecture of 16-bit Modified CSLA

The basic idea of Modified CSLA is to achieve lower power consumption with only slight increase in the delay. The main advantage of this BEC logic comes from the lesser number of logic gates then the n-bit Full Adder (FA) structure.

IV. BINARY TO EXCESS-1 CONVERTER (BEC) DESIGN

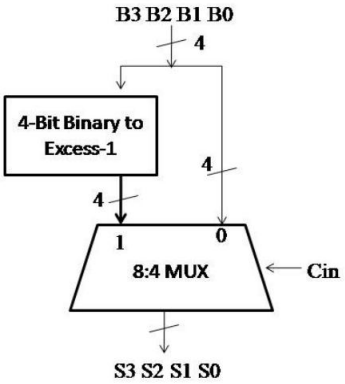

Fig. 3: 4-bit BEC with 8:4 MUX

A. Working Process of BEC

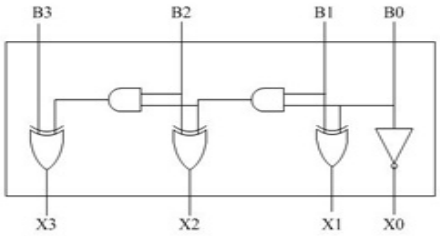

Fig.4:4-bit BEC[5]

Binary[3:0]	Excess-1[3:0]
0000	0001
0001	0010
0010	0011
1111	0000

Table 1: Function of 4-Bit Bec

X0= ~ B0
X1= B0 ^ B1
X2= B2 ^ (B0 & B1)
X3= B3 ^ (B0 & B1 & B2)

BEC block increments given binary input values by 1. The basic function of the CSLA is obtained by using the 4-bit BEC block together with the multiplexer as shown in Fig.3. 8:4 multiplexer gets one of input from RCA (B3, B2, B1, B0) and another input of from BEC block. Appropriate block of data is used to select either the BEC output or RCA output by multiplexer[3]. The architecture of 4-bit BEC block is shown in Fig.4, which can be modified for more/less number of bits.

V. 16-BIT CSLA USING D-LATCH

Further CSLA architecture can be modified by replacing BEC by D-Latch. Input carry of RCA structure is replaced by enable (clock) signal. When Clock clk=0, addition is performed (considering cin=0) which will be fed to D-Latch when clock signal becomes 1. Output of RCA block and D-Latch result is given to multiplexer.

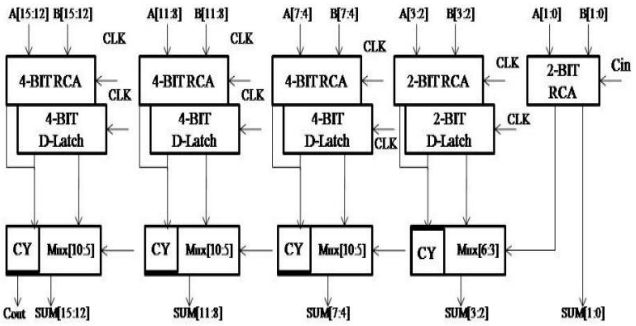

Fig. 5: Architecture of 16-bit Improved CSLA with D-Latch

Architecture of Improve 16-bit CSLA using D-Latch is shown in Fig-5, which is divided into five groups of different bit size RCA and D-Latch Block. First block consists of 2-bit RCA which provides direct sum and carry output bit. The subsequent 14-bits are divided into groups of (2+4+4+4) bit with RCA and D-latch block.

D-latch CSLA architecture provides lesser delay compared to CSLA with BEC, but overall area and power dissipation increased.

VI. SIMULATION RESULT

Table II exhibits comparison of the delay and power of various adders like Conventional CSLA, Modified CSLA, Improve CSLA using D-Latch for 8-bit, 16-bit, 32-bit, 64-bit. Different CSLA architecture is designed and implemented in Verilog language using Spartan3E family on Xilinx 13.2 ISE tools.

The 8-bit CSLA is done by the same structure of 16-bit CSLA except group 2 and 3. The 32-bit CSLA are divided into groups of (2+2+4+4+6+6+8) bit pattern, 64-bit CSLA are divided into groups of (2+2+4+4+6+6+8 +8+10+10+4) bit pattern. Using this different bit pattern to reduced the block and area of CSLA.

Word Size	Adder	Delay(ns)	Power(mw)
8-Bit CSLA	Regular (dual RCA)	11.083	157
	Modified (with BEC)	11.251	110
	Proposed (with D-Latch)	9.034	82
16-Bit CSLA	Regular (dual RCA)	15.405	153
	Modified (with BEC)	15.799	115
	Proposed (with D-Latch)	9.503	104
32-bit CSLA	Regular (dual RCA)	15.103	223
	Modified (with BEC)	20.794	222
	Proposed (with D-Latch)	13.575	127
64-bit CSLA	Regular (dual RCA)	20.488	361
	Modified (with BEC)	27.014	362
	Proposed (with D-Latch)	16.889	175

Table 2: Comparison of Different Types Of Adder

VII. CONCLUSION

The reduced number of gates of this work offers the great advantages in the reduction of area, total power and also reduces the delay. The Conventional CSLA has the disadvantages of more power consumption and occupying more area. The Modified CSLA reduced the area and power when compared to Conventional CSLA with increase in delay by the use of BEC converter. This paper shows a scheme which reduces the delay and power than conventional and modified CSLA by the use of D-Latch.

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