A Review on Pulse Triggered Flip-Flop with Conditional Pulse Enhancement Scheme

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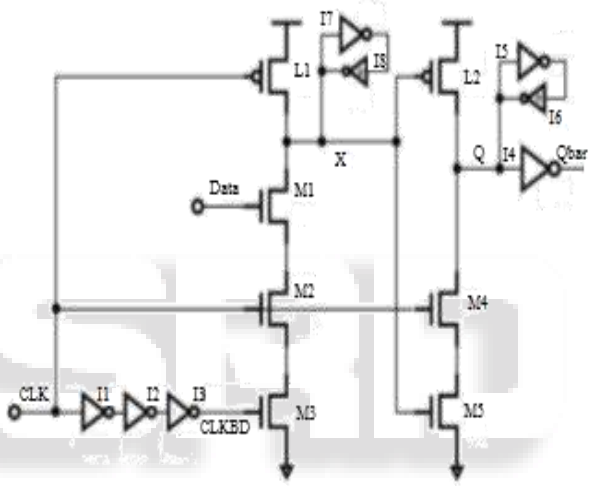
Abstract— In this review work, a low-power pulse-triggered flip-flop (PTFF) design is described. Conventional proposed Flip-Flop (FF) has two new features. First one, the pulse generation control logic and an AND function, is removed from the critical path to facilitate a faster discharge operation. To reduce the circuit complexity a simple two-transistor AND gate design is used. Second one, a conditional pulse-enhancement technique is devised to speed up the discharge along the critical path only when needed. As a result, transistor sizes in pulse-generation circuit and delay inverter can be reduced for power saving. Various post layout simulation results based on CMOS 90-nm technology reveal that the conventional proposed design features the best power-delay-product performance in three FF designs under comparison.

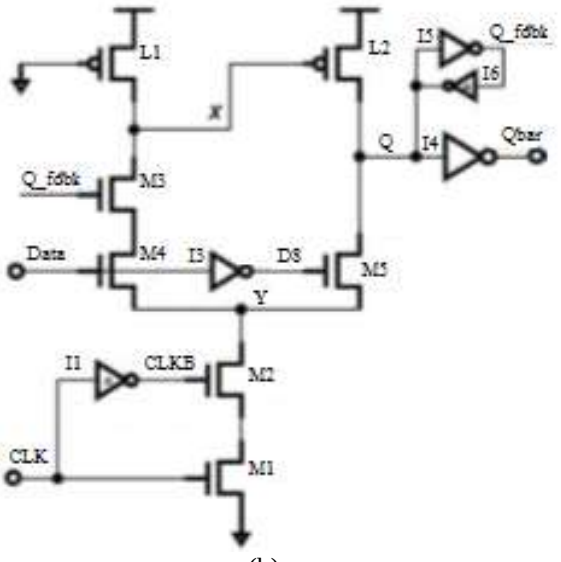
Key words: Flip-Flops, conditional pulse enhancement, low power, pulse triggered

I. INTRODUCTION

In current scenario the increasing significance of portable equipment need to limit power consumption and reduce heat dissipation, in very large scale integration chips. So that development of VLSI design places a major role in the complex systems. Where the complex system consists of analog, digital as well as memory elements and all this can be integrated on a single chip. For designing a circuit we come across many design metrics like low power, high speed and reduced the area of chip by considering the above design metrics a novel explicit Pulse triggered flip flop is designed. Flip flop are extensively used as a basic storage elements in a digital systems. The clock system composed of the clock interconnection network and timing elements, is one of the most power consuming components in a VLSI system. It accounts for 30%-60% of the total power dissipation in a system. FFs thus contribute a paramount portion of the chip area and power consumption to the overall system design. In this design a pulse triggered flip flop is preferred compare with the conventional transmission gate (TG) and master–slave predicated FFs in high-speed applications because pulse triggered flip flop is one which can execute in a single stage instead of two stages. A P-FF consists of a pulse generator for generating strobe signals and a latch for data storage. Sometimes the pulse triggered flip flop acts like an edge- triggered flip flop when there is a sufficient narrow latch is present. A P-FF is simpler in circuit entanglement. This results to a higher toggle rate for high-speed operations. P-FFs also allow time borrowing across clock cycle boundaries and feature a zero or even negative setup time. Pulse triggered flip flops are classified into two types based on their pulse generator used. They are implicit and explicit type pulse triggered flip flops. In implicit type of pulse triggered flip flop the pulse generator is present inside the flip flop where as in explicit pulse triggered flip-flop (ep-FF), the pulse is generated externally. Its power consumption and the circuit entanglement can be effectively reduced if one pulse generator is shares a group of FFs. This paper presents a novel low-power implicit-type P-FF design featuring a conditional pulse-enhancement scheme. Three additional transistors are introduced to support this feature. In spite of a slight increase in total transistor count, transistors of the pulse generation logic benefit from significant size reductions and the overall layout area is even slightly reduced. This gives rise to competitive power and PDP performances against other P-FF designs.



(a)



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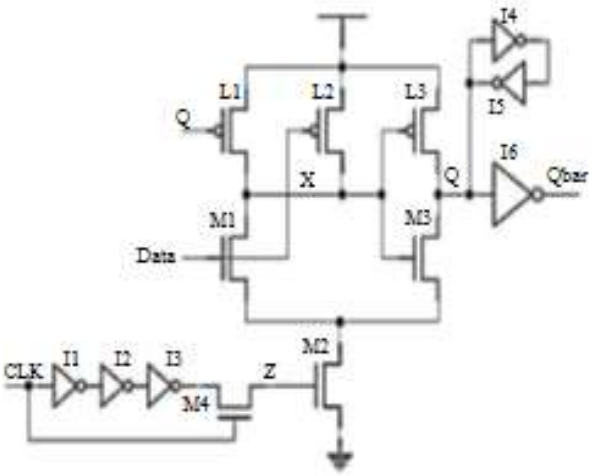

(c)

Fig. 1: Conventional pulse-triggered FF designs (a) ip-DCO (b) SCCER (c) MHLLF

II. Conventional FF Designs

A. Conventional Implicit-Type P-FF Designs

Some conventional implicit-type pulse flip-flop (P-FF) designs [1], which are used as the reference designs in later performance comparisons, are first reviewed. Fig. 1(a) shows P-FF design, named ip-DCO which contains an AND logic-based pulse generator and a semi-dynamic structured latch design. Both inverters I5 and I6 are used to latch data and inverters I7 and I8 are used to hold the internal node X. The pulse generator takes complementary and delay skewed clock signals to generate a transparent window equal in size to the delay by inverters I1-I3. There are two practical problems exist in this design. First one is, during the rising edge, NMOS transistors M2 and M3 are turned on. If data remains high or "1", node will be discharged on every rising edge of the clock. This leads to a large switching power. Second one is that node controls two larger MOS transistors (L2 and M5). The large capacitive load to node causes speed and power performance degradation.

Fig. 1(b) shows a refined low power pulse flip-flop (P-FF) design named SCCER using a conditional discharged technique [2]. In SCCER, the keeper logic (back-to-back inverters I7 and I8 in Fig. 1(a)) is replaced by a weak pull up transistor L1 in conjunction with an inverter I2 to reduce the load capacitance of node. The discharge path contains NMOS transistors M2 and M1 connected in series. In order to eliminate superfluous switching at node, an extra NMOS transistor M3 is employed. Since M3 is controlled by Q_fdbk, no discharge occurs if input data remains high or "1". The worst case timing of this design occurs when input data is "1" and node is discharged through four transistors in series, i.e., M1 through M4, while combating with the pull up transistor L1. A powerful pull-down circuitry is thus needed to ensure node can be properly discharged. This implies wider M1 and M2 transistors and a longer delay from the delay inverter I1 to widen the discharge pulse width.

Fig.1 (c) shows Modified hybrid latch flip-flop (MHLFF) [1][3]that have less no. of transistors due to its semi-latch structure. Internal node "X" is no longer pre-charged periodically by the clock signal but depend on the output and data. A weak pull-up PMOS transistor L1 controlled by the FF output signal Q is utilized to maintain the node X level at "1" or "high" when Q is "0"or "low". This design eliminates the nonessential discharging trouble at internal node X. However, it encounters a longer D-to-Q delay during "low" to "high" or "0" to "1" transitions because internal node X is not pre-discharged. NMOS transistors M2 and M3 are required to enhance the discharging ability of the output. There is another drawback with this design is that internal node X becomes floating when input Data and output Q both are equal to "1" or "high".

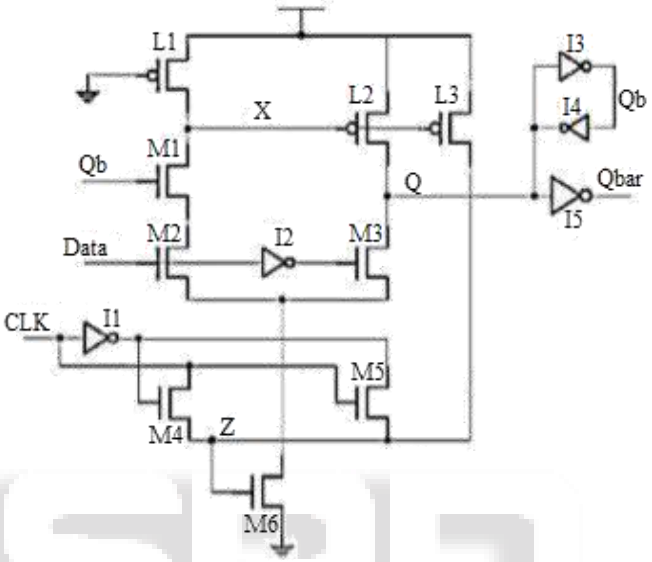

Fig. 2: Conditional pulse enhancement scheme FF [1]

B. Conventional Proposed FF Design

Fig. 2 shows a conditional pulse enhancement scheme FF [1] design. Here in this design, longest discharging path is formed when input data is "high" or "1" while the Qb output is also "high" or "1". An extra PMOS transistor P3 is added at the top, to enhance the discharging under this condition. This PMOS transistor is normally turned off because most of the time node X is pulled high. After the rising edge of the clock, the clock delay inverter drives output node back to zero but with little delay. Due to this a clock pulse is generated and the generated clock pulse is taller in height, which enhances the pull-down strength of lower NMOS transistor M6 which is responsible for the discharging. When the clock has reached to logic "1" or "high", then lower NMOS transistor M6 is turn off due to no clock pulse. Due to this voltage level of node X rises and turns off upper PMOS transistor L3 eventually. With the help of extra PMOS transistor L3, the width of the generated discharging pulse is stretched out. This creates a pulse with sufficient width for correct data requirement, a bulky delay inverter design, which comprises most of the power consumption in pulse generation logic, is no longer required. It should be noted that this conditional pulse enhancement technique takes effects only when FF output is subject to a data change from 0 to 1 or low to high. This leads to low power consumption in the FF circuit and also reduces the leakage power due to shrunken transistors in the discharging path.

III. SIMULATION RESULTS

In this review paper, we have simulated all results at 90nm technology with 1V power supply at 500MHz CLK frequency. A load of 20fF is used in the simulation process. Table I shows the comparison of the power and delay. It is clear from the table that conditional pulse enhancement FF shows the better results w.r.t. other FFs described in the [1].

Flip – Flops	**ipDCO**	**MHLFF**	**SCCER**	**Conditional pulse enhancement FF**
No. of transistors	23	19	17	19
D-to-Q delay (ps)	131.20	175.43	134.05	123.56
Power (100% switching activity) uW	32.33	30.64	28.21	25.38
PDP (fF)	4.24	5.37	3.78	3.13

Table 1: Comparison Table of different conventional FF designs

IV. CONCLUSION

In this review paper, we simulated low-power pulse-triggered FF design by employing two new design measures. The first one successfully reduces the number of transistors stacked along the discharging path by incorporating a PTL-based AND logic. The second one supports conditional enhancement to the height and width of the discharging pulse so that the size of the transistors in the pulse generation circuit can be kept minimum. Simulation results indicate that the conventional proposed design excels rival designs in performance indexes such as power, D-to-Q delay, and PDP.

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