Implementation of Vedic Multiplier using VLSI
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Abstract—Today’s processors mostly depend on multipliers as it is the important key hardware block in processors. This paper proposed the design of 64x64 bit Vedic multiplier based on Urdhava Tiryakbhyam sutra which means vertical and crosswise. The multiplier and multiplicand each group in 32 bit which decomposes the use of 32x32 multiplication module. Further, the Verilog coding Urdhava Tiryakbhyam sutra for 64x64 Vedic multiplier have been done using Xilinx ISE 14.2 software.

Key words: Urdhva-Tiryagbyham, Vedic multiplier and sutras, Digital signal processor, Xilinx

I. INTRODUCTION
Arithmetic operations mostly depend on multipliers. Multipliers based operations such as MAC and computation Intensive Arithmetic Functions (CIAF) used in DSP application such as FFT, convolution and filtering. DSP execution time depends mostly on multiplier, so there is a need of high speed multipliers. The demand for high speed multipliers has been increased due to expanding computer and signal processing application. High speed multipliers can over come time delay and power consumption results into optimize at design level. This optimization includes design and implementation, digital circuit, topology and circuit style and Algorithm that are being implemented.

II. HISTORY OF VEDIC MATHEMATICS
Vedic Mathematics is an ancient mathematics technique used in trigonometry, geometry, factorization, quadratic equation and even in calculus. Bharati Krishna Tirthaji maharaja (1884-1960) combined his all study in Vedic mathematics and gave explanation of its various applications. He proposed 16 sutras (formula). The sutras are not a wonder but are logical Vedic Mathematics technique is being used worldwide.

The word Vedic means temples of “Knowledge”. The 16 sutras are as follows
1) (Anurupye) Shunyamanyat
2) Chalana-Kalanabhyam
3) Ekadhikina Purvena
4) Ekanyunena Purvena
5) Gunakasamuchyah
6) Gunitasamucchah
7) Nikhilam Navatashcaramam Dashatah
8) Paraavartya Yojayet
9) Puranapuranabhyam
10) Sankalana-vyavakalanabhyam
11) Shesanyankena Charamen,
12) Shunyam Saamyasamuccaye
13) Sopaantyadvayamantyam
14) Urdhva-Tiryagbyham

III. URDHYA TIRYAGBHYAM SUTRA
The design of multiplier is based on udhyta Tiryaghyam sutra. This sutra has been used for multiplication of two decimal numbers. Urdhva Tiryagbyham sutra means vertically and crosswise. This sutra is applicable for all cases of multiplication. It is based on concept through which generation of all partial products are added concurrently. In this technique as the no. of bits increases the complexity, delay increases very slowly. Hence it is time efficient.

IV. THE PROPOSED MULTIPLIER ARCHITECTURE
The architecture of 32x32 and 64x64 bit Vedic multiplier are designed below. The architecture is based on Urdhaya Tiryagbyham sutra which means vertical and crosswise. The advantage of Vedic multiplier is partial and addition is done simultaneously. Thus it reduces time delay.

A. Vedic Multiplier for 32x32 bit
The 32x32 bit Vedic multiplier module is implemented by using four 16x16 Vedic multiplier module. Lets analyze 32x32 say A=A31 to A0 and B=B31 to B0. The output lines will be S=S63 to S0. First lets divide A into Ai and Aii where Ai=A15 to A0 and Aii=A31 to A16. Similarly B=Bi and Bii where Bi=B15 to B0 and Bii=B31 to B16. After multiplication of this four blocks result is passed to 33 bit adders to get 64 bit out. The architecture is shown below. Example:
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Fig: Architecture of 32x32 bit Vedic multiplier

B. Vedic Multiplier for 64x64 Bit

Similarly as for 32x32 bit 64x64 is implemented by using four 32 bit multiplier. A is decomposed into Ai and Aii and B into Bi and Bii. Where Ai=A31 to A0 and Aii=A63 to A32 similarly Bi=B31 to B0 and Bii=B63 to B32. The result of four multipliers is passed to 65 bit adders to obtained 127 bit output.

V. DESIGN VERIFICATION AND SIMULATION

In this paper 32x32 and 64x64 bit Vedic multiplier is designed in Verilog logic synthesis and simulation is done in Xilinx ISE 13.4 project navigator and I sim simulator integrated in the Xilinx package.

A. Simulation Results

After the successful execution the RTL view is generated in fig a and b. Fig c shows simulation results.

Fig a. RTL Schematic of 32x32 Vedic multiplier
B. Simulation Results of 32 x32 Vedic Multiplier

Fig. b: Internal RTL Schematic of 32x32 Vedic multiplier

1) 64x64 Vedic Multiplier:

Fig.: RTL Schematic of 64x64 Vedic multiplier

Fig: Internal RTL Schematic of 64x64 Vedic multiplier
VI. CONCLUSION

This paper presents the efficient way of multiplication using Vedic Mathematics. Vedic multiplication using Urdhaya sutra been successfully executed and simulated and found number of adders required is less compared to conventional adders.

REFERENCES