Low Power & Area Efficient Carry Select Adder

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Abstract— In the field of electronics, adder is a digital circuit that performs addition of numbers. To perform quick arithmetic operations and functions, carry select adder (CSLA) is one of the quickest adder used in many data processing processors. The structure of CSLA is such that there is further scope of reducing the area, delay and power consumption. Simple and efficient gate – level modification is used in order to reduce the area, delay and power of CSLA. Based on the modifications, 8-bit, 16-bit, 32-bit and 64-bit architectures of CSLA are designed and compared. In this paper, conventional CSLA is compared with Modified Carry select adder (MCSLA), Regular Square Root CSLA (SQRT CSLA), Modified SQRT CSLA and Proposed SQRT CSLA in terms of area, delay and power consumption. The result analysis shows that the proposed structure is better than the conventional CSLA. Carry select adder (CSLA) is one of the fastest adder in comparison to all other adders. This review undergoes very simple and efficient gate-level modification to reduce the area and delay of the CSLA. Based on this modification, 8-bit, 16-bit, 32-bit and 64-bit Square-Root CSLA (SQRT CSLA) architecture have been developed having comparison with the regular SQRT CSLA architecture. The proposed circuit design has reduced area and delay as compared with the regular SQRT CSLA.

Key words: CSLA, RCA, BEC

I. INTRODUCTION

The designs of area and high-speed data path logic systems are the most important areas of research & study in VLSI system design. In electronic system and applications adders are mostly used. As we know that in microprocessors, one can perform millions of instructions per second. So, the speed of operation is most important factor to be considered while designing multipliers. Even in servers and personal computers (PC), power dissipation is an important design parameter. In today's era, the designs of area-efficient and power-efficient high-speed logic systems are one of the crucial areas of research in VLSI design. In digital adders and circuit design, the speed of addition is limited by the time required by carry to propagate through the adder. In recent years, the increasing demand for high-speed arithmetic units in micro-processors, image processing units and DSP chips has paved the path for development of high-speed adders as addition is an important operation in almost every arithmetic unit, and it too acts as the general building block for synthesis of all other arithmetic computations. Ripple Carry Adders have most compact design but they are having slow speed of operation. Whereas, the Carry Look Ahead Adder has fast speed but it consumes more area. Carry Select Adder solves both the problem as generated by that of the Ripple Carry Adder and Carry Look Ahead Adder. A Carry-Select Adder can be structured by using a single Ripple-Carry Adder and an add-one circuit rather than using the dual Ripple-Carry Adders. Based on the area, delay and power consumption requirements, several adder structures have been proposed. A multiplexer-based add-one circuit is proposed to reduce the area with less speed penalty. This acts as the sum for each bit position in an adder which is generated serially only after the previous bit position has been summed and a carry is propagated to the next position.

The CSLA is used in many calculation systems to avoid the problem of carry propagation delay by independently generating multiple carries and then select a carry to generate the sum. However, the regular or conventional CSLA is not area efficient as it uses multiple pairs of Ripple Carry Adders (RCA) to generate partial sum and carry by taking carry input $C_{in} = 0$ and $C_{in} = 1$,where the final sum and carry are selected by the multiplexers.

The basic idea of this work is to use Binary to Excess-1 Converter (BEC) rather than that of RCA with $C_{in} = 1$ in the regular CSLA to obtain lower area and delay. As, in BEC logic, lesser number of logic gates are used and hence the circuit is optimized, the modified CSLA is more efficient than that of the regular CSLA.

II. LITERATURE SURVEY

Much of the research efforts of the past years in the area of digital electronics have been directed towards increasing the speed of digital system. There are different types of fast adders used in processors such as Ripple Carry Adder (RCA), Carry Look Ahead Adder (CLA) and Carry Select Adder. Ripple carry adder generates the compact design but their computation time is high. Carry Look Ahead Adder basically provides fast result but it results in increase in area. Carry Select Adder provides a better approach between RCA and Carry Look Ahead Adder. Ripple Carry Adder generates worst case delay, because it comprises of N single bit full adders. Each adder gives the sum and carry. The carry generated by the previous full adder is given as the input to the next adder. The carry is transferred through every stage and produces a delay which is called as a worst case delay. In Ripple Carry Adder, as value of N increases, delay also increases. Vitit Kantabutra et.al, 1993 [1] proposed a model of a very fast adder which was an improvement on Spanning Tree Carry Look ahead Adder (henceforth STCLA), also known as the Redundant Cell Adder. Hiroyuki Morinaka et.al, 1995 [2] proposed a model of carry select adder structure by considering the trade-offs between speed and area.

Hiroshi Makino et.al, 1996 [3] proposed a model which has high speed redundant binary (RB) architecture, and was optimized for the fast CMOS parallel multiplier. Keshab K. Parhi et.al, 1999 [4] proposed a model which presents novel hybrid carry select modified-tree (CSMT) adder architectures for binary carry generators and adders using multiplexers only. Yuke Wang et.al, 2002 [5] proposed a model which presents a general architecture for designing hybrid carry-look ahead/carry–select adders. Amaury Neve et.al, 2004 [6] proposed a model which presents method to minimize the power-delay product of 64-

bit carry-select adders intended for high-performance and low-power applications.

Dilip P. Vasudevan et.al, 2007 [7] proposed a model that encodes the sum bits using two-rail codes; the encoded sum bits are then checked by self-checking checkers. Yajuan He, et.al, 2008 [8] proposed a model in which there was an efficient reverse converters for transforming the redundant binary (RB) representation into two's complement forms. Padma Devi et.al, 2010 [9] proposed a model in which power dissipation is one of the most important design objectives in integrated circuits, after speed. Samiappa Sakthikumaran et.al, 2011 [10] proposed a model of Carry Select Adder (CSLA) which was known to be the fastest adder among the conventional adder structures.

Sajesh Kumar U. et.al, 2012 [11] proposed a model of High performance digital adder with reduced area and low power consumption is an important design constraint for advanced processors. B. Ramkumar et.al, 2012 [12] proposed a model of Carry Select Adder (CSLA), one of the fastest adders used in many data-processing processors to perform fast arithmetic functions.

III. RIPPLE CARRY ADDER (RCA)

Ripple carry adder is a logical circuit using multiple full adders to add N-bit numbers. In a simple Ripple Carry Adder, the C_{out} of each stage is the C_{in} of the next stage. The sum and the output carry of any stage cannot be produced until the carry input occurs which causes a time delay in the addition process. The carry propagation delay for each full adder as shown in Fig. 1 is a time from the application of the input carries until the output carry occurs. It is suggested that the adder has a regular layout and uses 5 logic gates per bit. For an n bit adder total number of logic gates used is 5n and the delay is 2n+2 logic gates. For area calculation only two input AND, OR and XOR gates are considered.

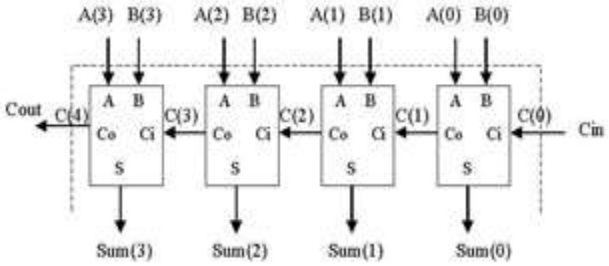

Fig. 1: Four-Bit Ripple Carry Adder.

The Ripple Carry Adder [1]–[2] is used for evaluating addition of two N-bit numbers. For addition of N-bit numbers, N full adders are needed. From the second full adder carry input of every full adder is the carry output of its previous full adder. This kind of adder is stated as Ripple Carry Adder because of rippling of carry to next full adder is governed here. The general structure of full adder is shown in Fig. 2.

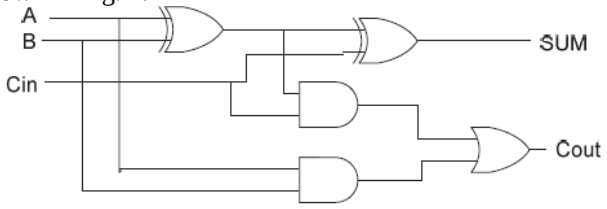

Fig. 2: Basic Diagram of Full Adder

Using the equation C_{in} = Gn-1+Pn-1Cn-1, conventional Ripple Carry Adder is structured. Here each stage uses the output of the previous stage. The delay is directly proportional to the number of bits as shown in Fig. 3. This adder undertakes the minimum number of logic gates and the worst case delay is generally more.

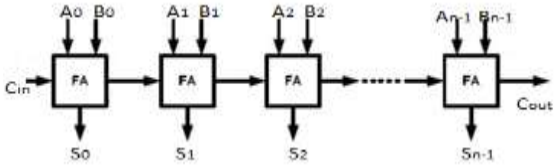

Fig. 3. Block Diagram of Four-Bit Ripple Carry Adder

The model of a ripple-carry adder is simple, which allows for fast design time; however, the ripple-carry adder is relatively slow, since each full adder must wait for the carry bit to be calculated from the previous full adder. The gate delay can easily be calculated by inspection of the full adder circuit.

IV. BINARY TO EXCESS - 1 CONVERTER (BEC)

As stated above the main idea of this work is to use BEC instead of the RCA with C_{in}=1 in order to reduce the area and power consumption of the regular CSLA. The structure and the functionality of a Four-bit BEC is shown in Fig. 4. The next figure i.e. Fig. 5 illustrates how the basic function of the CSLA is obtained by using the Four-bit BEC together with the Mux. One input of the 8:4 Mux gets as it input (B3, B2, B1 & B0) and another input of the Mux is the BEC output.

This produces the two possible partial results in parallel and the Mux is used to select either the BEC output or the direct inputs according to the control signal C_{in}. The importance of the BEC logic stems from the large silicon area reduction when the CSLA with large number of bits are designed. The Boolean expressions of the 4-bit BEC is listed as (note the functional symbols! NOT, &AND, ^XOR):-

X0 =! B0
X1 = B0^B1
X2 = B2^ (B0 & B1)
X3 = B3^ (B0 & B1 & B2)

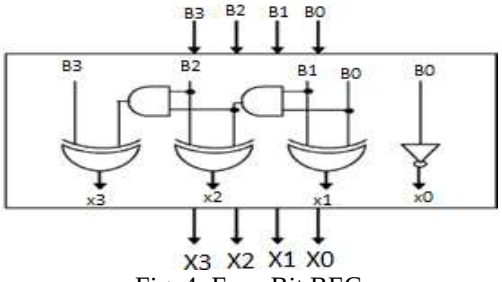

Fig. 4: Four-Bit BEC

The number of bits required for BEC logic is 1 bit more than that of the RCA bits. The modified block diagram [12] is also divided into various groups of variable sizes of bits with each group having the ripple carry adders, BEC and corresponding Mux. Thus, the sum 1 and carry 1 (output from Mux) are depending on Mux and results computed by RCA and BEC respectively. The sum 2 depends on carry 1 and Mux. For the remaining parts the arrival time of Mux selection input is always greater than the arrival time of data inputs from the BEC's.

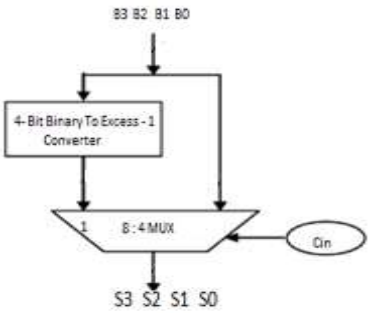

Fig. 5: Four-Bit BEC with 8:4 MUX.

V. CARRY SELECT ADDER

Carry Select Adder is a fast adder which is used in digital communication and Memory Architectures as shown in Fig. 6. The Carry of one ripple carry adder will be '0' and another will be '1'.Here the output sum and carry is identified by the 2 to 1 multiplexers. The control signal of the multiplexer can be represented by carry (C_{in}).

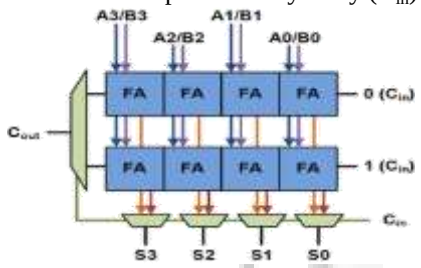

Fig. 6: Basic Carry Select Adder Circuit

The Carry Select Adders are divided into two types: Uniform sized adders and variable sized adders. When the bit length is equally divided it is stated as an uniform sized adder. It is also called as the linear Carry Select Adder. In variable sized adders the bit lengths are generally unequally divided. It is also called SQRT Carry Select Adder (CSLA). Normally the CSLA is designed with the dual Ripple Carry Adders with the carry being '1' and '0'. Here, rather than that of having dual ripple carry we are having only single ripple carry adder while the binary to excess one converter is connected instead of RCA with Carry '1' [8]-[12].

The block diagram of conventional Carry Select Adder (CSLA) [12] is shown in Fig. 7. CSLA uses RCA to generate sum and carry values using initial carry as 0 and 1 respectively, before the actually carry arrives in. Upper RCA is given with carry initial value as logic "0" while lower RCA is given with carry initial value as logic "1". Multiplexer selects the result of carry "0" path if the previous carry is logic '0' or the result of carry "1" path if the previous carry is logic '1' i.e. actual carry is used to select the sum and carry using a multiplexer.

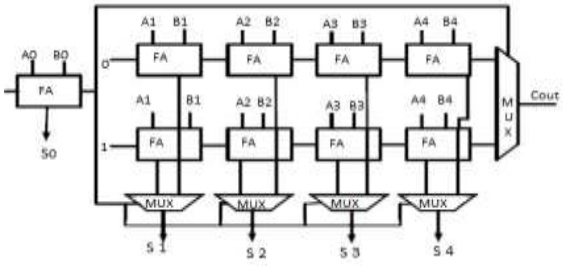

Fig. 7: Block Diagram of Conventional CSLA.

VI. GATE LEVEL ANALYSIS

The adder block using a Ripple carry adder, BEC and Mux is described in this section. In this, we explain the delay & area using the theoretical approach and show how the delay and area effect the total implementation. The delay and area evaluation methodology considers all gates to be made up of AND, OR, and Inverter, each having delay of 1 unit and area of 1 unit as shown in Fig. 8.

We can then add up the number of gates in the longest path of a logic block that contributes to the maximum delay. The XOR gate can be implemented by using the NAND Gate as shown in Fig. 9.

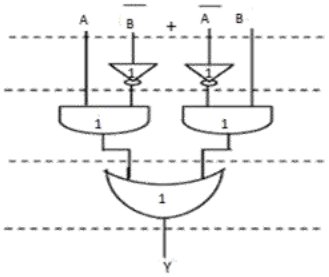

Fig. 8: Delay and Area Evaluation of XOR.

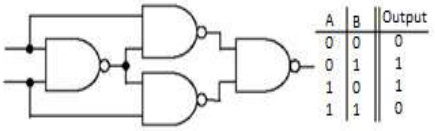

Fig. 9: XOR Gate and its Truth Table.

To replace the n-bit RCA, n+1 bit BEC logic is required as shown in Fig. 10. BEC using carry out is shown in Fig. 11.

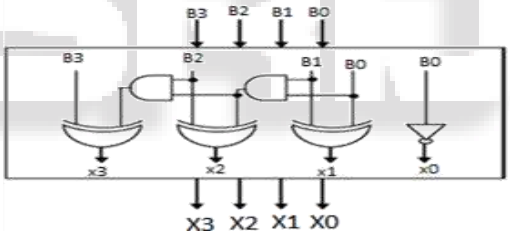

Fig. 10: Four-Bit Binary to Excess-1 Converter

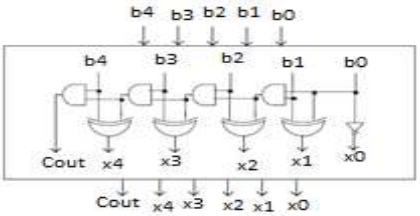

Fig. 11: Four-Bit Binary to Excess-1 Converter Using Carry Out.

The CMOS Representation of AND Gate is shown in Fig. 12. In digital electronics, a NAND gate (negative-AND) is a logic gate which produces an output that is false only if all its inputs are true; thus its output is complement to that of the AND gate. A LOW (0) output results only if both the inputs to the gate are HIGH (1); if one or both inputs are LOW (0), a HIGH (1) output results. It is made using transistors. By De Morgan's theorem, AB=A+B, a NAND gate is equivalent to inverters followed by an OR gate. The NAND gate is significant because any Boolean function can be implemented by using a combination of NAND gates. This property is called functional completeness.

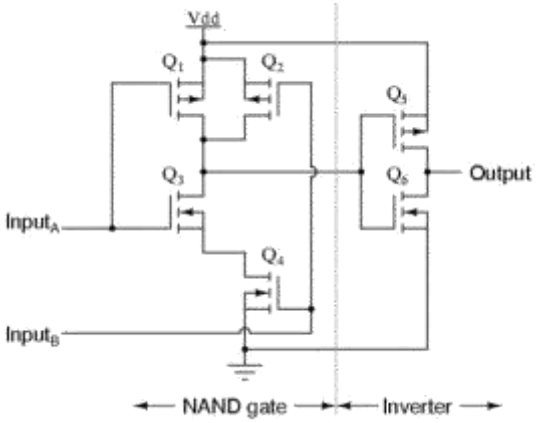

Fig. 12: CMOS Representation of AND Gate.

The CMOS Representation of NAND Gate is shown in Fig. 13.

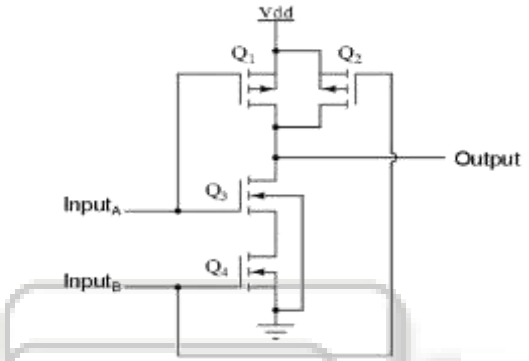

Fig. 13: CMOS Representation of NAND Gate.

In the modern approach, we use the universal gate i.e. NAND Gate instead of the basic gate i.e. AND Gate. Due to this use, the number of gate count reduces as when we implement the CMOS Design of the basic gate, we require 22 total number of Gates but, when we use the universal gate for the BEC Design, the CMOS model contains 16 total number of Gates.

Hence, the circuit becomes more optimized and thus, its area decreases. Consequently, the delay as well as Leakage, Switching & Internal Power also reduces. Hence, the final generated modified model of the Carry Select Adder with the help of the modified BEC is Low Power as well as Area efficient. XOR gate is logically explained as shown in Fig. 14.

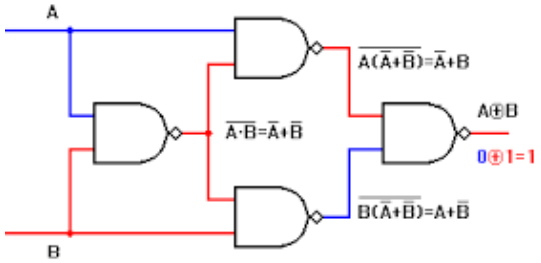

Fig. 14: Implementation of XOR Gate with NAND Gate.

VII. Regular & Modified 16-bit Sqrt. CSLA

The structure of the 16-bit regular SQRT CSLA is shown in the Fig. 15.

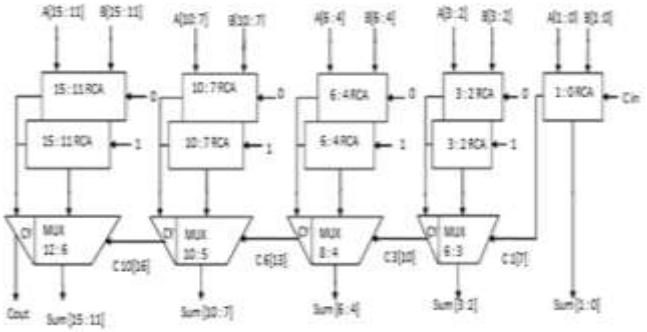

Fig. 15. Regular 16- Bit CSLA Model.

The structure of the modified 16-bit regular SQRT CSLA [12] is shown in the Fig.16.This modified model includes the BEC instead of RCA which is used in the Regular Model of CSLA.

The Regular model of CSLA uses the upper as well as lower blocks of RCA whereas; the modified model of CSLA uses RCA as well as the BEC model.

The upper blocks contain RCA model whereas, the lower blocks contain the BEC based model. The newly generated model is hence efficient in design. The truth table of 4- Bit BEC is shown in Table I.

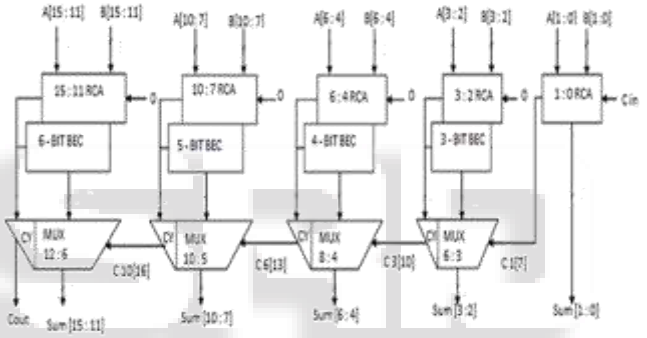

Fig. 16: Modified 16- Bit CSLA Model.

Table I explains the binary logic as B1, B2, B3 & B4 in the L.H.S. whereas their corresponding Excess-1 Logic as E0, E1, E2 & E3 respectively.

Table II shows the Regular as well as the Modified model of the CSLA and hence the parameters such as area, delay & leakage power.

Hence, there is the scope to make CSLA more area and power efficient by optimizing the circuit. Also, a trade-off can be made between area consumption as well as the leakage power.

Binary Logic B0 B1 B2 B3	Excess-1 Logic E0 E1 E2 E3
0000	0001
0001	0010
0010	0011
0011	0100
0100	0101
0101	0110
0110	0111
0111	1000
1000	1001
1001	1010
1010	1011
1011	1100
1100	1101
1101	1110
1110	1111
1111	0000

Table 1: Truth Table of 4- Bit Bec

Word Size (Bits)	Adder	Delay(ns)	Area(μm^2)	Leakage Power(µW)	Area-Delay Product (10^{-21})
8-Bit	Regular	1.719	991	0.007	1,703.5
	Modified	1.932	880	0.004	1,700.16
16-Bit	Regular	2.775	2,272	0.017	6,304.8
	Modified	3.022	1,901	0.011	5,744.822
32-Bit	Regular	5.137	4,783	0.036	24,570.2
	Modified	5.427	3,914	0.016	21,241.27
64-Bit	Regular	9.174	9,916	0.075	90,969.3
	Modified	9.501	8,102	0.043	76,977.102

Table 2: Comparison Table of The Regular [12] & Modified Sqrt Csla

VIII. CONCLUSION & FUTURE WORK

Power, delay and area are the main performance parameters of CSLA and the reduction of these parameters is the challenging issue of today's VLSI research. But as we can analyze from the recent method proposed that there is a trade-off between area consumption and delay of CSLA. Therefore, there is a scope to make CSLA more delay and area efficient by optimizing the circuit. The overall improvement in Modified CSLA shows better results in terms of area power and delay. Hence, proposed modified CSLA is being used for power and area efficient devices. Further, it will be interested to design the higher bits of CSLA such as 128 bit and hence calculate its parameters based on the modified design.

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