Built in Self-Test Technique Based on Three Weight Pattern Generation

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Abstract— Built-In Self-Test (BIST) techniques are used to find solution to the difficult problem of testing VLSI systems and circuits. Key vector monitoring simultaneous BIST scheme used to avoid problems in online and in offline BIST schemes. A original key vector monitoring simultaneous BIST architecture has been presented and SRAM-cell are used to store the information of whether an key vector has appeared or not during normal operation. The proposed method is three weight pattern generation pseudorandom built-in-self-test (BIST) method to achieve complete fault coverage in BIST applications by reducing number of vectors. Weighted sets are 0, 1, and 0.5 have been used generate test pattern generation and achieve low testing time less power consumption, The proposed scheme is simulated and synthesized using Xilinx 12.1 software.

Key words: Built-In-Self-Test, Concurrent Testing, On-Line, Off-Line

I. INTRODUCTION

Built-In-Self-Test (BIST) techniques provide an attractive solution to test modules deeply embedded in complex integrated circuits. BIST technique reduces the product development cycle and cost-effective system maintenance .BIST utilizes a Test Pattern Generator (TPG) to generate the test patterns which are applied to the Circuit under Test (CUT). BIST are classified into off-line BIST and on-line BIST. In offline BIST the normal operation of the CUT is stalled in order to perform test. To avoid this performance degradation input vector monitoring have been proposed with exploit input vectors arriving at the input of the CUT during the normal operations [2-10].

The block diagram of an input vector monitoring concurrent BIST architecture is shown in fig1.The CUT has n inputs and m outputs and it is tested exhaustively; Hence the test size is N=2n.The technique can operate in either normal or test mode, depending on the value of the signal T/N. In fig 1 mux is used to select whether the mode ii test mode or normal mode depending on the value of T/N.

If T/N=0 then the mode is normal mode, if T/N=1 then the mode in test mode. During the normal mode A[n:1] input is get by the mux and the same input is applied to CUT and CBU(Concurrent BIST Unit),the input is applied to the CBU is compared to the applied test vectors if any matches exists between these two inputs then hit occurs. If hit occurs the input is removed from the applied test set and the corresponding response is observed in the Response Verifier (RV).

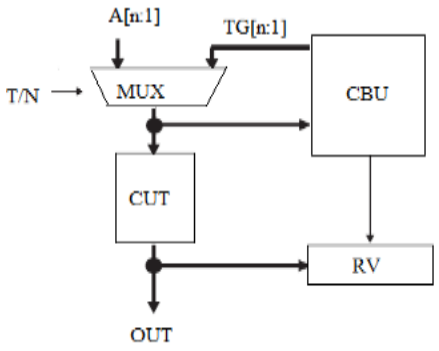


Fig. 1: Concurrent BIST Architecture

During the test mode output of CBU is applied as input to the CUT. In order to calculate the time required for the test during the normal mode the CTL (Concurrent Test Latency) schemes in used. The brief is organised as follows. In section II, we introduce the literature review and in Section III, we introduce the proposed approach. In Section IV, summarizes the simulation results. Finally Section V summarizes the conclusion of this brief.

II. LITERATURE REVIEW

In the conventional off-line method uses Test Pattern Generator (TPG) and fault simulation algorithms to find test set vectors. This test vectors is used to find the fault, test vectors can be applied externally or from the chip which already stored in it. The test vectors that is applied from the chip during the test phase is called off-line BIST technique. Four types of test pattern is used in BIST. They are exhaustive, pseudo-exhaustive, pseudo random pattern generator and deterministic.

In exhaustive testing, test pattern generator and fault models are not required and also not required to store the test vectors in the chip, here the test pattern generated by LFSR (Linear Feedback Shift Register) with nonlinear circuitry added to include all zero pattern. This method cannot be used for large number of inputs since it takes more time for testing the circuit. To overcome these disadvantages pseudo exhaustive testing [4], verification testing[5] and testing using random inputs[6] can be used. The above mentioned method give high hardware overhead .To reduce the hardware overhead for systems where it continuous functioning is of utmost importance, online concurrent testing is the only solution.

III. ARCHITECTURAL OVERVIEW

Let us consider the combinational circuit that has n inputs shown in fig 2 which can generate 2^n possible test vectors. The proposed method based on the idea of monitoring input vectors every times it checks the occurrence of hit, when test vectors are matched with input if hit occurs then the RV in enabled. The applied input vectors are subdivided into two

groups, higher order (H) and lower order(L) bits respectively.

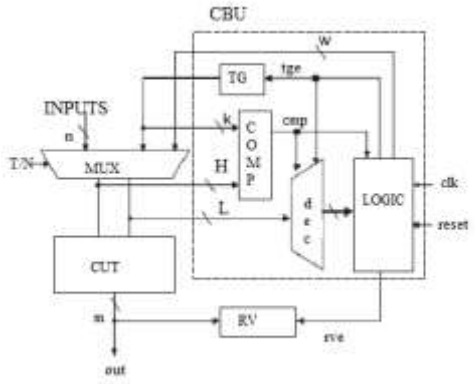


Fig. 2: Proposed Architecture

Higher order bits is used to check whether the input has been into consideration. Low order bits is used to identify the location of the incoming input vectors. The proposed architecture is shown in fig 2. In this architecture T/N signal is used the mode of operation. When T/N=0 the architecture operates in normal mode that time the normal input is applied to CUT and the same input is applied to the CBU as higher order and lower order bits. The higher order bits are applied to the one input of the comparator and the other input is applied from the TG output. The lower order bits are applied to the decoder.

Fig 3 shows the operation of the modified decoder of proposed architecture it operate as follows, when tge signal is enabled all the outputs of the decoder is enabled. When cmp is disabled all the outputs of the decoder is disabled, when tge is disabled and cmp is enabled the module operates as normal decoder.

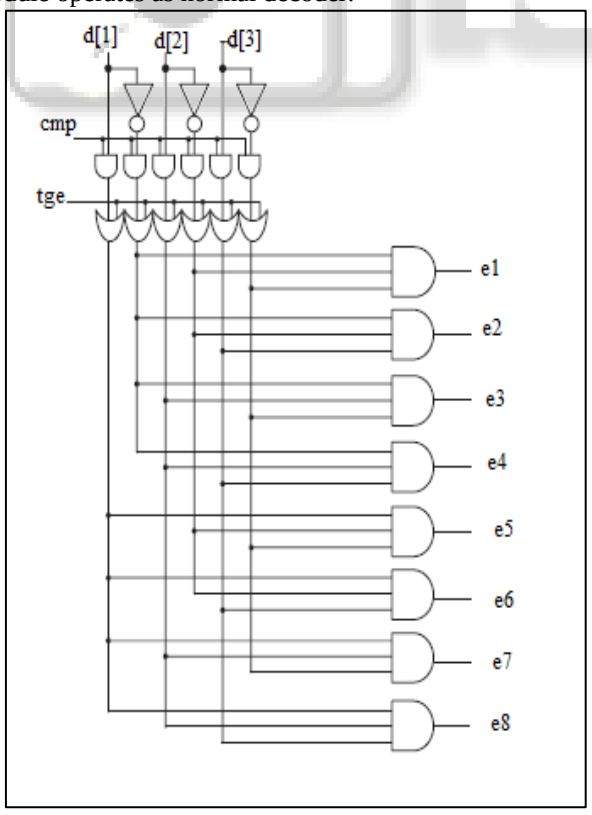


Fig. 3: Modified Decoder Circuit Used In Proposed Architecture

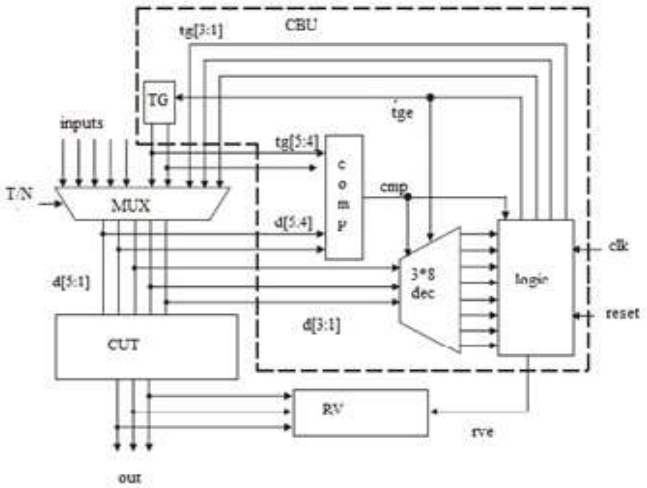


Fig. 4: Proposed Architecture for n=5, w=3, and k=2

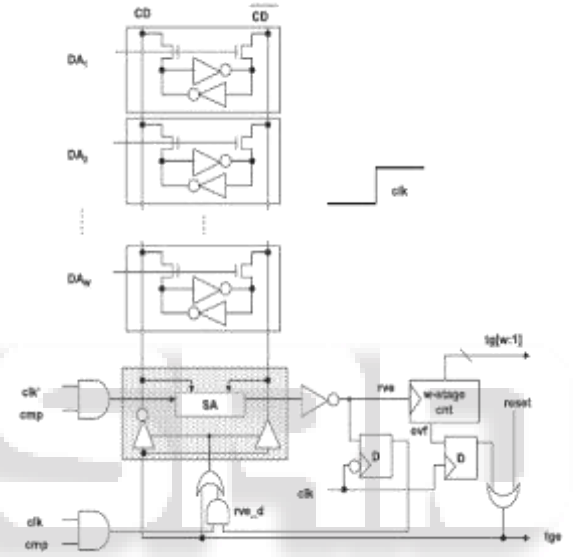


Fig. 5: Logic Module of the Proposed Architecture

The logic module of the proposed architecture is shown in fig 5. It consists of group of cells, sense amplifier, flip-flop and w-stage counter .The logic module is used to store the test vectors. The counter drives the tge signal through unit flip-flop delay. By using the clock signal the clk and clk' is enabled. We describe the operation of logic module, presenting the following cases: 1) reset of the module; 2) hit of the vectors 3) tge operation.

A. Reset of the Module:

The reset signal is applied to the module. After the reset signal is applied because of this the tge signal is activated and the output of all the decoder is enabled. (Fig 3)

B. Hit of Vector:

The same set of input is applied to both CUT and CBU, TG in the CBU generates the test vectors for the applied input. The higher order bits of the normal input is given to comparator, test vectors generated by TG is applied as another input of the comparator. The comparator compares both the input if there is a match hit occurs then cmp is enabled. If there is no hit then tge signal is enabled.

C. Tge operation:

When all the cells are full, then the value of the *w*-stage counter is all one. Hence, the activation of the rve signal

causes the counter to overflow; hence in the next clock cycle(Through the unit flop delay) the tge signal is enabled and all the cells(because all the outputs of the decoder of Fig. 3 are enabled) are set to zero. When switching from normal to test mode, the *w*-stage counter is reset. During test mode, the *w*-bit output of the counter is applied to the CUT inputs. The outputs of the counter are also used to address a cell. If the cell was empty (reset), it will be filled (set) and the RV will be enabled. Otherwise, the cell remains full and the RV is not enabled.

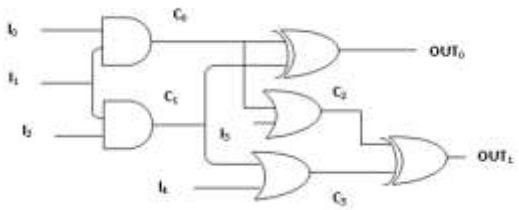


Fig. 6: CUT of the Proposed Architecture

The Circuit Under Test(CUT) of the proposed architecture is shown in fig 6.In existing system during the test mode the generated test vector is applied to the i_0,i_1,i_2,i_3,i_4(output from Mux) and the corresponding response is capture by RV. Each applied vector consumes some amount of power. To reduce the power consumption the proposed method uses the 1st three bits are same such that 101 so the value of C_0, C_1 and OUT_0 are not altered and the output is determined by only $I_3$and I_4 value. This will reduce the power compared to the existing method and also simulation is carried out for both the good and fault circuit.

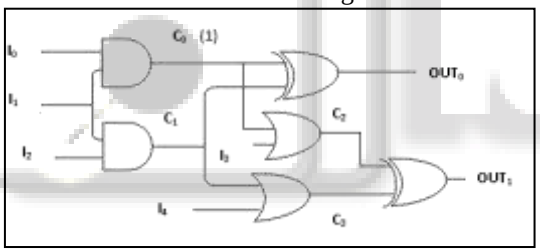


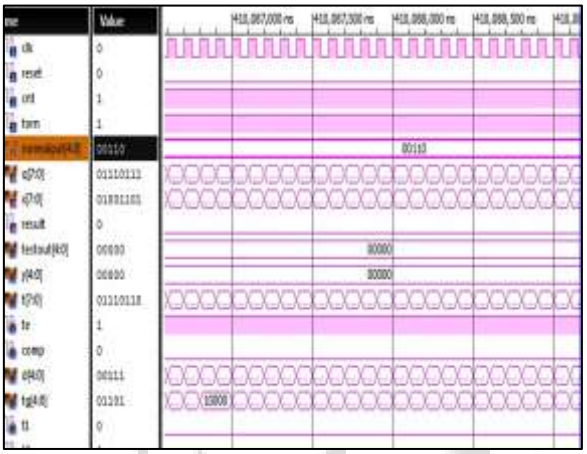
Fig. 7: Fault Circuit

In fig 7 c0(1) represents the struck-at-1 fault that is always the c0 value is 1.during the simulation the simulation results is compared with the memory if match is not occur then this will produce the result=1 else it will produce 0.if 1 is produced then the circuit is faulty otherwise it is fault free circuit

IV. SIMULATION RESULTS

A) Existing Method Output

B) Fault Circuit Output



C) Proposed CUT Output

V. COMPARISON

Methods	Power consumption
Existing Method	14mw
Proposed Method	12mw

Table 1:

VI. CONCLUSION

.A novel input vector monitoring concurrent BIST architecture presented here is based on the use of a SRAM-cell whose structure is for storing the information of whether an input vector has appeared or not during normal operation. Input vector monitoring concurrent BIST scheme thus overcomes problem appearing separately in online and in offline BIST schemes .The proposed method is a weighted Pseudo-random built-in-self-test (BIST) scheme utilized in order to drive down the number of vectors to achieve complete fault coverage in BIST applications. Weighted sets comprising three weights, namely 0 and 1 have been successfully utilized so far for test pattern generation, since they result in both low testing time and low consumed power. The proposed scheme is simulated and synthesised using Xilinx 12.1 software.

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