Self-Bias Transistor & Transmission Gate Logic Technique: for 8:1 Multiplexer

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Abstract— Power dissipation and propagation delay are the contradicting factors in the design of VLSI CMOS devices. This paper aims at reducing power and energy dissipation using Transmission Gate Logic (TGL) Multiplexer CMOS circuits and Self Bias Transistor Circuits comprise of reducing the power supply voltages to investigate the performance parameters i.e. delay, power for the combinational circuit using power reduction techniques and compare them to find out the best one. These techniques can be used further for various applications in the field of VLSI design. A competitive approach is applied to the 8 Bit MUX circuit emphasizing on the minimum Power-Delay trade-off and minimum Transistor count. The PMOS and NMOS transistors are connected together for strong output level. SBT technique achieves 70% reduction of power dissipation and TGL technique achieves 83% reduction of power in active mode as compared to the conventional CMOS design. SPICE Simulations are performed with 0.18µm CMOS technology.

Key words: Self Bias Transistor (SBT), Transistor Gate Logic (TGL), Low Power, Delay

I. INTRODUCTION

The semiconductor industry has witnessed an explosive growth of integration of sophisticated multimedia-based applications into mobile electronics gadgetry since the last decade. As the CMOS process technology shrinks, it has driven the VLSI industry towards very high integration density and system on chip designs.

According to the International Technology Roadmap for Semiconductors (ITRS), leakage power dissipation may eventually dominate total power consumption as technology feature sizes shrink. While there are several process technology and circuit-level solutions to reduce leakage in processors, The idea to enhance the performance of logic circuits results in the development of many logic design techniques during the last two decades. The paper makes an effort to increase prominence for transporting the signals from input to the output and wishes to limit power consumption. The developments include transportable device applications requiring low power consumption and high output because of their little chip size with large density of elements, redoubled complexity.

Multiplexer abbreviated as MUX can be analogue circuits using MOSFETs and transistors or they can be of digital type circuits made from logic gates [1]. MUX are used in a number of applications which includes digital signal processing, telephone network, communication system and telephone memory etc. Transmission gate type of MUX structure implemented using very less number of transistors compared to CMOS based logic design [6]. Pass transistor logic is used to improve the performance of arithmetic and logic circuits. It reduces the count of transistors used to make different logic gates, by eliminating redundant transistors and it also uses less number of transistors, runs faster, and requires less power than the same function implemented with the same transistors in CMOS logic [10]. An 8:1 Multiplexer may be the basic building block of the “switch logic”. The Multiplexer circuit often wants to combine eight or a lot of digital signals onto one line, by inserting them there at totally different times. Technically, this can be referred to as time-division multiplexing.

The various methods are widely used for reducing power dissipation in circuits, reducing switching activities, supply voltages and load capacitances [8]. Many leakage reduction techniques have area unit which cut back leakage power within the circuit to a significant level. Self-Biasing Transistor has become one amongst the foremost widely used circuit design techniques for reducing leakage current in power dissipation [7]. This paper concentrates on reduction of leakage power that happens throughout the transition within the circuitry. This paper designs low power 8:1 Multiplexer using various CMOS designs like pass semiconductor device, transmission gate and Self Biasing Technique. The Multiplexer has been realized with SBT & TGL power reduction technique in 180 nanometer technology [4] [10].

II. MULTIPLEXER

A multiplexer (or MUX) is a device that selects one of several analog or digital input signals and forwards the selected input into a single line. A multiplexer with 2^n inputs has n select lines.

A 8:1 Multiplexer has eight sets of input I(0), I(1), I(2), I(3), I(4), I(5), I(6), I(7) and three select lines S (0), S (1) and S (2) and a single output OUT. The equation for the output signal is

\[ \text{OUT} = \sum_{i=0}^{7} \text{S}(i) \cdot I(i) \]

(1)

Fig. 1: Conventional 8:1 MUX
A. Self-Bias Transistor (SBT) Based 8:1 Mux

A Self Bias Transistor (SBT) is one which has its gate and drain connected together and works as a current-controlled switch. The gate voltage is provided by the drain and MOSFET is always in saturation. As long as a MOS transistor is in saturation region, the current is independent of the drain voltage and it behaves as an ideal current source seen from the drain terminal [7]. The current through a long channel device in saturation is given by equation

\[ I_{dsat} = \frac{1}{2} K_n (V_{GS} - V_{th})^2 \]  

(2)

And for very short channel devices is given by

\[ I_{dsat} = W \cdot V_{sat} \cdot C_{ox} (V_{GS} - V_{th}) \]  

(3)

Where \( K_n = K'_n (W/L) \) is the gain factor and \( K'_n = \mu C_{ox} \) is the process transconductance of the device. \( V_{GS} \) is the gate to source voltage and \( V_{th} \) is the threshold voltage of the transistor. \( V_{sat} \) is the saturation voltage in short channel device. The working of SBT is controlled by the current in the branch where SBT is connected [4] [7].

For the short-channel devices \( V_{GS} \) is proportional to \( I_{ds} \). Thus by controlling the current through the SBTs we can control the charging and discharging of the load capacitance and hence the dynamic power dissipation which is due to charging and discharging of the capacitor.

\[ C = \frac{1}{V_{DD}} \int I \, dt \]  

(4)

\[ P_{dyn} = CV_{DD}^2 \]  

(5)

Fig. 2: Schematic of (a) NMOS SBT (b) PMOS SBT

B. Transistor Gate Logic (TGL) Based 8:1 Mux

The transmission gate can be used to quickly isolate multiple signals with a minimal investment in board area and with a negligible degradation in the characteristics of those critical signals. A transmission gate is defined as an electronic element that will selectively block or pass a signal level from the input to the output. The CMOS Transmission Gate uses Transmission Gate Logic to appreciate advanced logic functions employing a little range of complementary transistors. It solves the matter of low logic level using PMOS as well as NMOS [8].

Transmission gate has a switch with low resistance and capacitance having ratio less logic. Also, DC characteristic of this gate is independent of input levels. It is designed by connecting each source to source and drain to drain terminal of NMOS and PMOS transistors. Because the NMOS transistor is passing strong signal ‘0’ and PMOS transistors passes strong signal ‘1’ towards the output [3] [9].

Fig. 3: SBT Based 8:1 MUX

Fig. 4: Transmission Gate

Table 1: Truth Table for A Transmission Gate

<table>
<thead>
<tr>
<th>S</th>
<th>IN</th>
<th>OUT</th>
</tr>
</thead>
<tbody>
<tr>
<td>H</td>
<td>H</td>
<td>H</td>
</tr>
<tr>
<td>H</td>
<td>L</td>
<td>L</td>
</tr>
<tr>
<td>L</td>
<td>X (Don’t Care)</td>
<td>Z (High Impedance)</td>
</tr>
</tbody>
</table>

Fig. 5: TGL Based 8:1 MUX
When the voltage on node S is a Logic 1, the complementary Logic 0 is applied to node active low S, allowing both transistors to conduct and pass the signal at IN to OUT. When the voltage on node active low S is a Logic 0, the complementary Logic 1 is applied to node A, turning both transistors off and forcing a high impedance condition on both the IN and OUT nodes. The schematic diagram includes the arbitrary labels for IN and OUT, as the circuit will operate in an identical manner if those labels were reversed. This design provides true bidirectional connectivity without degradation of the input signal [2] [6] [9].

III. SIMULATION RESULT
The Simulation result is measured by Tanner EDA tool. Here the result of Self Biased Transistor Based & Transmission Gate Logic (TGL) Multiplexer has been calculated.

![Simulation Waveforms](image)

Fig. 4: Simulated Waveforms For Logic 111

A. Comparison Results

<table>
<thead>
<tr>
<th>Parameters</th>
<th>SBT</th>
<th>TGL</th>
</tr>
</thead>
<tbody>
<tr>
<td>Power(µW)</td>
<td>36.5</td>
<td>19.8</td>
</tr>
<tr>
<td>Delay(n.sec)</td>
<td>14.5</td>
<td>4.08</td>
</tr>
<tr>
<td>Transistor Count</td>
<td>110</td>
<td>34</td>
</tr>
</tbody>
</table>

Table 2: Comparison b/w Parameters

IV. CONCLUSION
This paper designs an 8:1 Multiplexer with Self Bias Transistor & Transmission Gate Logic for reduction of leakage power and leakage current. The Transmission Gate Logic (TGL) using 34 transistors while SBT uses 110 transistors. Power dissipation and Delay of TGL Technique is less as compared to (SBT). The result calculates in active mode with a fixed VDD. The 8:1 Multiplexer was designed using 180nm technology on Tanner EDA tool. Using this tool the results have been calculated. Power of 8:1 MUX using SBT is 36.5 µW and Transmission Gate Logic (TGL) is 19.8µW. The Delay of Self bias Technique is 14.5ns and Transmission Gate Logic (TGL) is 4.08ns.

REFERENCES