Efficient Interleaver Design for MIMO-OFDM Based Communication Systems on FPGA

Shridevi Kenganal[1] Dr.M.A.Goutham[2]
[1]M. Tech Student [2]Professor
[1,2]Department of Electronics and Communication
[1,2]AIT, Chikkamagaluru

Abstract— A memory-efficient and faster interleaver implementation technique for MIMO-OFDM communication systems on FPGA. The IEEE 802.16 standard is used as a reference for simulation, implementation, and analysis. The main aim is to design interleaver for various modulation schemes like BPSK,QPSK,16QAM,64 QAM. The interleaver plays a important role in improving performance of EFC codes.The interleaver design is divided in to two parts as address generator and interleaver memory.The finite state machine baesd interleaver shows the better performance like maximum frequency and FPGA resources utilization as compared previous FPGA techniques. Interleaver is implemented using xilinix ISE and simulation results are presented The hardware model is implemented on FPGA kit spratan 3

Key words: MIMO-OFDM, FPGA

I. INTRODUCTION

The IEEE developed some standards for the mobile broadband wireless access.The gradual increase in use of internet makes the quest of BWA and it provides the alternative solution to Digital Subscriber Line (DSL) orcable modem for Internet access. WLAN and WiMAX are two important standard for wireless communication system.Ihe orthogonal frequency multiplexing technique is used in the WLAN and WiMAX standard in order to reduce the inter symbol interference over wireless channel.The different modulation schemes like BPSK,QPSK,16QAM,64QAM are used to generate address in the interleaver system.The interleaver is used in the communication system to minimize the effect of burst errors and to improve the performance of EFC codes in wireless channel Orthogonal Frequency Division Multiplexing technique offers promising solution that has gained tremendous research interest isn recent years due to its high transmission capability and also for alleviating the adverse effects of Inter Symbol Interference (ISI) and Inter Channel Interference (ICI). Orthogonal frequency-division multiplexing (OFDM) is a method of encoding digital data on multiple carrier frequencies OFDM is popular due to its multi-path interference, and mitigate inter-symbol interference (ISI) causing bit error rates in frequency selective fading environments The Interleaver is used to enhance the error correcting capabilities of block of codes.The block interleaver has different interleaving pattern for different code rates and modulation schemes used in the the WiMAX system. The main function of block interleaver sytem is to rearranges the encoded symbols over multiple code blocks and that effectively spreads out long burst noise sequences so that they appear as independent random symbols errors to the decoders.

II. RELATED WORK

An efficient technique to model convolutional interleaver using a hardware description language and it is implemented on field programmable gate array (FPGA) spartan kit.The technique utilizes embedded shift register of FPGA chip to implement incremental shift register in the interleaver. Software simulation of the model are presented.[1].The proposed technique reduces consumption of FPGA resources to a large extent as compared to conventional implementation technique using flip-flop. This implies that proposed technique has a lower power consumption and reduced delay in the interconnection network of the FPGA. This technique is also reduces wastage of memory as scompared to memory based implementation technique for digital audio broadcasting (DAB) application.

The 8 bit and 32 bit version of interleaver as well as deinterleaver is impelemated .The two implementation technique are different because they involve full FPGA based design and that leads to less resource requirement.It makes lesser power consumption and interconnect delay. The proposed technique shows saving of FPGA resources above 81 % as compared to conventional technique using flipflops.The delay in the interconnection network is reduced inside FPGA because of Use of lesser slices.For digital audio broadcast (DAB) application,the memory wastage is reduced by 30.38% The 8 bit convolution interleaver is implemented and tested on Xilinx Spartan-3 (device X400.It has total 896 numbers of configurable logic blocks (CLBs) arranged in 32 X 28 matrix manner.

The 8 bit and 32 bit convolution interleaver – deinterleaver is implemented and tested on Xilinx Spartan 3 FPGA kit.The VHDL model of Convolutional interleaver_deinterleaver pairs (both 8 bit and 32 bit) are implemented and tested into Xilinx Spartan-3 (Device: XC3S400) FPGA platform. A comparative analysis of the FPGA resource requirement in the delay units of interleaver and deinterleaver taken together for the two implementations: with and without SRL16 for both 8 bit and 32 bit version.

The proposed technique saves 50% and 81% FPGA resources as compared to implemenattiontechnique without SRL16 FOR 8 bit and 32 bit respectively.The proposed technique reduces dealy in the interconnection network inside fpga and it also reduces power consumption too.

III. IMPLEMENTATION

The proposed hardware model of WiMAX interleaver consists of two sections: address generator and interleaver memory as shown in Fig. 2 .Conventional block interleaver uses two memory blocks out of which one memory block is written and the other is read based on the value of select (SEL) signal. The design the memory block has dual port

internal memory module of FPGA by partitioning it into two sub-modules.

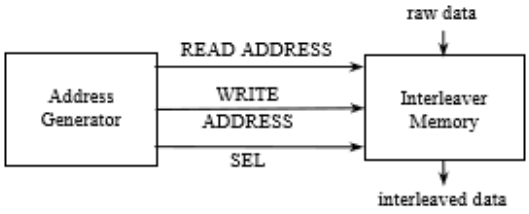

Fig. 2: Top level view of WiMAX interleaver

The address generator circuit contains the stages of multiplexers that implements equal or unequal increments for different modulation schemes like BPSK,QPSK,16 QAM,64 QAM.The address generator circuits generate the read addresses ,write addresses,sel signals.The design contains three levels of multiplexers.The level mux consists of 8 multiplexers.top most four mux for 16QAM and bottom four mux for 64QAM respectively.The selection of topmost mux in first level is controlled by t flip-flop and bottom four mux in first level controlled by mod-3 counter.

The level two consists of three multiplexers. Topmost mux consists of eight input lines.The input to second and third mux are from first level mux outputs of 16qam and 64 qam respectively.In level two topmost multiplexer is used for BPSK.The second and third mux in level 2 are used for 16 QAM and 64QAM

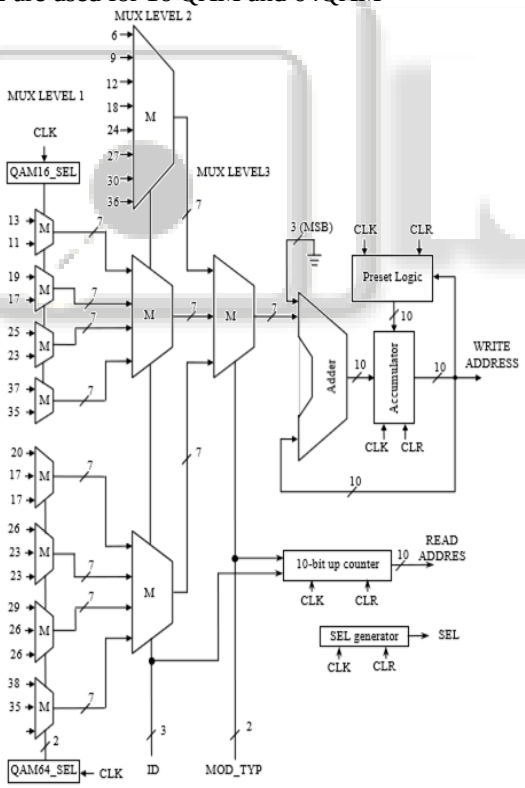

Fig. 3: Address generator of interleaver

The output of level two mux are passed to level three mux based on MOD_TYP.The level three mux has 7-bit output and that acts as a one input to 10-bit adder circuit after zero padding.The other input to the adder is form accumulator that holds previous address.The after addition new address is written in the accumulator. The circuit operation begins with CLR=1and which resets accumulator,preset logic circuits, sel signal generator and read address generator as shown in fig 3. The first address generated is always zero. In the first clock event sum of mux output and previous content of accumulator is that is stored in the accumulator(zero) ,which is the second address of the interleaver. The subsequent clock events generate the consective addresses of the of the interleaver by adding present output of accumulator with constant value chosen by the muxs.The read address are generated using 10 bit up counter as shown in fig 3.1 The 10 bit up conuter is reset when counter reaches to terminal count for ID and desired modulation For example, in case of 16-QAM with Ncbps = 288, the counter counts from 0 to 287 and then repeats.The SEL signal is switches between write and read memory block and it is basically t flip-flop.The SEL signal is initialized to zero using CLR input. The preset logic as a finite state machine and the principal function is to generate beginning write addresses for all iterations

The design has two more signals generated by preset logic that are start signal and select signal.The start signal provides pulse signal to QAM16_SEL and QAM64_SELwhen the addresses reach to the terminal value of the iteration.The start signal provides correct functionality of the interleaver.A select signal from preset logic is used as a input for sel signals and generation of read addresses.The select signal provides pulse signal at the end of one complete Ncbps.The select signal has the advantages as ,circuitry used in read addresses and sel signal signal generator become simpler.

The interleaver memory block has two memory modules (RAM1 and RAM2) and three muxs ,an inverter as shown in figure 4.In block interleaving one memory block RAM-1 is used to write over and other one RAM-2 is used to read and vice-versa.RAM-1 and RAM-2 memory module receives either write address or read address with the help of mux connected to their address inputs and SEL line.At the beginning RAM-1 receives read address and RAM-2 gets write address with help of WE(write enable) signal of RAM-2 active.After particular memory block is read or written to the desired location the status of SEL line changes and it performs the reverse operation. The mulitiplexers are used in the circuit and that provides correct read address,write address.The inverter is used to provide correct write and read enable signal

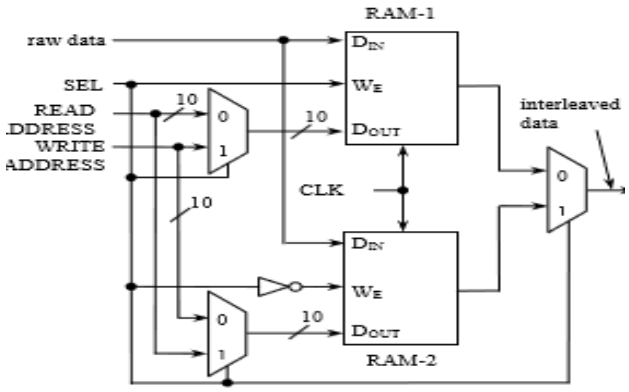

Fig 4: schematic view of interleaver memory block

IV. RESULTS

The simulation results are in the form of timing digram using ModelSim Xilinx Edition-III version 6.0a software.The simulation results for bpsk,qpsk,16 qam,64 qam is as shown in fig 5,fig 6,fig 7 and fig 8.

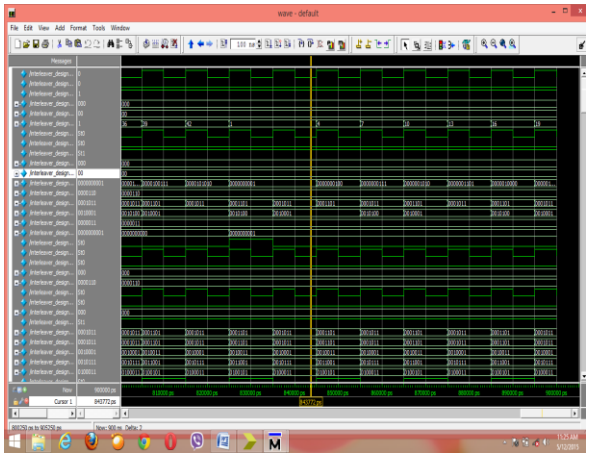

Fig. 5: simulation results for BPSK

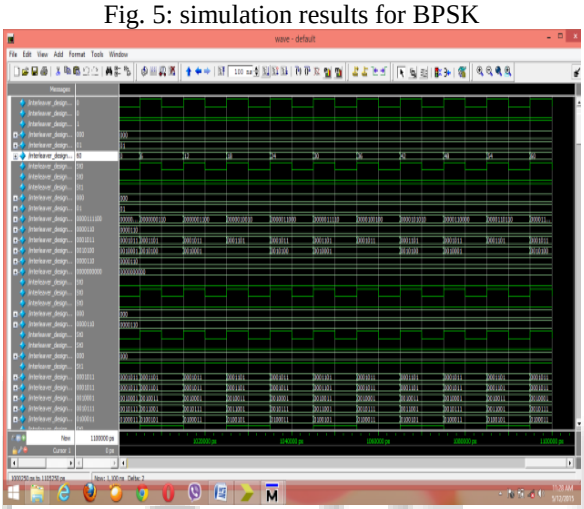

Fig. 6: simulation results for QPSK

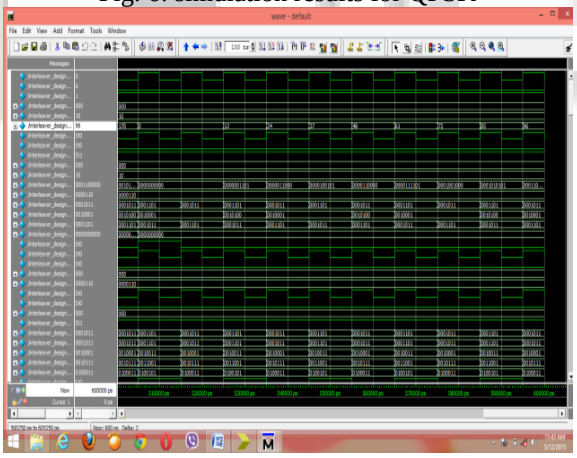

Fig. 7: simulation results for 16QAM

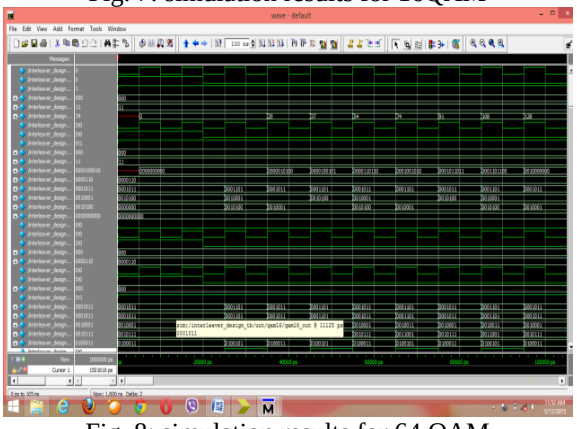

Fig. 8: simulation results for 64 QAM

V. CONCLUSION

A full FPGA implementation of WiMAX multimode interleaver. It proposes a novel finite state machine based address generator used for generation of write and read addresses for the interleaver memory. The interleaver memory is implemented using dual port Block RAM of Xilinx Spartan-3 FPGA. The presented circuit supports all the code rates and modulation schemes permitted under IEEE 802.16e standard. The simulation results endorse the correct operation of both address generator and interleaver as a whole. The novelty of our approach includes higher operating frequency and better resource utilization in FPGA.

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