VLSI Implementation of 64 Bit PCS Generator Using Non Linear Feedback Shift Register in Communication Systems

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Abstract— Spread Spectrum is wireless communication in which the baseband data is spread over the entire available bandwidth. In the project, data spread is done by Pseudo Chaotic Sequences (PCS). Spread Spectrum is mainly used to overcome the interference problems associated with data transfer systems and to deliver a heightened secure transmission of data. In the project, we specify the design and implementation of Direct Sequence Spread Spectrum (DSSS) system with PCS generator. The prototype is generation of 64-bit Chaotic sequences and implementing DSSS system with generated sequences. The length of spreading sequences is extended and the auto correlation and cross correlation properties are verified for the generated sequences. The low cross correlation value reveals that performance of DSSS system with Chaotic sequences is comparatively better than conventional PN sequences.

Keywords: Spread Spectrum, Pseudo Chaotic Sequence, Pseudo Noise sequence, Direct Sequence Spread Spectrum

I. INTRODUCTION

Spread Spectrum (SS) has been defined as a means of transmission in which the baseband data is spread over the entire available bandwidth. It is a form of wireless communications in which the transmitted signal frequency is varied deliberately. Theband spread at the transmitter is accomplished by utilizing a code which is independent of the data and at the receiver de-spreading is accomplished by the same code and hence the data recovery with synchronized reception in the system.

There are different types of spread spectrum in which Direct Sequence Spread Spectrum is widely recognized technology. Spreading code is generated using the DSSS. Intentional and non-intentional interference can be resisted by spread spectrum. If single user is considered then Spread Spectrum Multiple Access is not bandwidth efficient. However since many users are sharing the spectrum and bandwidth without interfering, this technique becomes bandwidth efficient in the environment of multiple users. Advantages of Spread Spectrum (SS) are as follows:

1) Reduced interference: In SS systems, interference from undesired sources is considerably reduced due to the processing gain of the system.
2) Security from eavesdropping: Since the applied codes are unknown to hostile user, it is not possible to detect the message of another user.
3) Low power spectral density:As the signal is spread over a large frequency-band, the Power Spectral Density is getting very low, so other communications systems do not suffer from this kind of communications.
4) Low susceptibility to multi-path fading: Because of its inherent frequency diversity properties, a spread spectrum system offers resistance to degradation in signal quality due to multi-path fading. This is particularly beneficial for designing mobile communication systems.
5) Immunity to jamming: An important feature of spread spectrum is its ability to withstand strong interference, sometimes generated by an enemy to block the communication link. This is one reason for extensive use of the concepts of spectrum spreading in military communications.
6) Random access possibilities: Start of transmission can be done at any arbitrary time by the users.

Spread spectrum techniques for digital communication were initially developed for military applications because of their high security and their susceptibility to interference from other interceptors,as in [1]. Now days spread spectrum techniques are being used in variety of commercial applications such as mobile and wireless communication, as in [1]. Compared to Frequency hopping and Time hopping SS systems, direct sequence SS system is more efficient system. DSSS is the most commonly used form of Spread Spectrum communication in which narrow band information signal is converted into a wider band (spread) signal or spreading of the narrow band signal is achieved by means of its direct multiplication to a high bit rate spreading sequence, as in [3]. DS-SS systems are simpler to implement, low probability of interception and can withstand multi-access interference reasonably. Even though frequency-hopping devices use less power and are cheaper, but the performance of DS-CDMA systems is usually more reliable. Hence, in this paper we are dealing only with Direct Sequence Spread Spectrum System. The spread spectrum is accomplished by spreading codes like PN sequences, Pseudo random sequences. These sequences are generated by linear feedback shift registers which limit the length of sequences. The auto correlation and cross correlation properties are not up to mark for these sequences. Therefore, a special type of spreading sequence called Pseudo Chaotic Sequence has been introduced which are more flexible sequences. The important properties of these sequences are sensitive to initial conditions and they cannot be predictable since the sequences are generating from non-linear feedback shift register (NLFSR). These Pseudo Chaotic Sequences can be used an economical alternative spreading codes to all the sequences generated by Linear Feedback Shift Register such as PN sequences, M-sequences, Gold sequences and Kasami sequences.

II. DIRECT SEQUENCE SPREAD SPECTRUM SYSTEM

There exists many techniques for accessing multiple users simultaneously in to the spread spectrum communication system. The available multiple access techniques are Frequency Hopping Spread Spectrum (FHSS), Time Hoping Spread Spectrum (THSS) and Direct Sequence Spread Spectrum (DSSS) technique. Compared to Frequency Hopping and Time Hopping Spread Spectrum systems, Direct Sequence Spread Spectrum system is more efficient system. Because DS-SS systems are simpler to implement, low probability of interception and can withstand multi-access interference reasonably. Also the number of users are not limited in DSSS whereas in FHSS and THSS have limited number of users. DSSS can also be operated very well in the presence of strong co-channel interference. Considering the advantages of Direct Sequence Spread Spectrum over other multiple access techniques, Direct Sequence Spread Spectrum is the chosen technique in the project for designing the system model in the spread spectrum communication medium using the special spreading codes called Pseudo Chaotic Sequences.

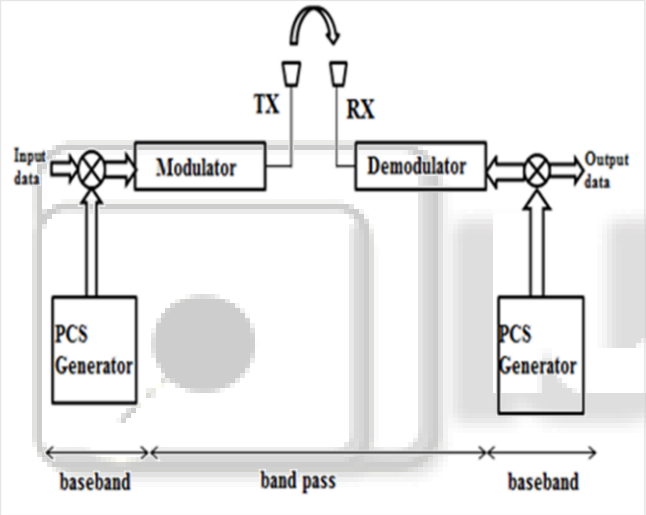

Fig. 1: DSSS system block diagram

Fig.1 shows the block diagram of DSSS system. It consists of PCS generator, modulation block, demodulation blocks, transmitter and receiver sections along with the communication channel, input and output data. Direct Sequence Spread Spectrum involves spreading of data over entire available bandwidth by converting narrowband data into wideband data at the transmitter section. This wideband data is received at receiver section and is converted back to narrowband and thus recovery of original baseband data. PCS generators present in both modules of transmitter and receiver sections are synchronized using initial key to create exact sequences. At the beginning of communication, spreading code is assigned to transmitter and receiver sections and each bit of baseband data is translated to that code before modulation. Then the data is spread in the communication medium. At the demodulator, inversion has done using the same key to retrieve the output data.

III. GENERATION OF PSEUDO CHAOTIC SEQUENCES

Usually in Spread Spectrum communication, the sequences used are periodic wherein a sequence of 1's and 0's repeats itself exactly with a known period. The commonly used periodic PN sequences are m-sequences. Which require simple instrumentation in the form of a Linear Feedback Shift Register (LFSR). But these shift registers limit the length of PN sequences. Therefore, Non Linear Feedback Shift Register (NLFSR) is used to generate Pseudo Chaotic Sequences. The block diagram of NLFSR is as shown in the Fig.2.

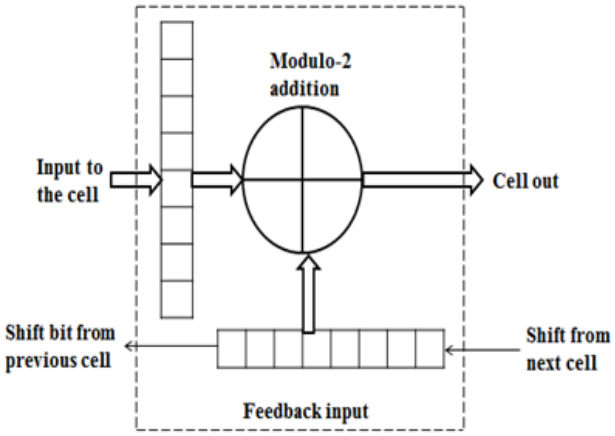

Fig. 2: Cell structure of basic NLFSR

The basic non-linear feedback shift register cell consists of two 8-bit programmable registers and XOR function block. Initial condition is given to both the registers. While at initial phase, input registers are loaded with different values which constitutes different PCS generator for different users. For every key generation, the input to the cell is forwarded by the previous cell output and feedback register is filled with previous cell feedback. At every cell, Modulo-2 addition is performed on each bit values of two registers and the output taken as cell out which is also of 8-bit. The feedback register creates the nonlinearity in the code generation. This NLFSR cell is cascaded to obtain the Pseudo Chaotic Sequence pattern of required length. In paper [1] the length of sequences obtained from PCS generator are of length 32-bit and used four NLFSR cells in cascade for the generation of 32-bit sequences. We can increase the period of sequence and the number of users by increasing the number of cells and size of registers. Since the number of implementation possibilities are very high due to just changing only initial condition programmability, this new system of sequence is inherently more difficult to intercept, as in [1].

A. Proposed architecture of PCS generator

In the proposed system, the length of sequences generated by PCS generator is extended from 32-bit to 64-bit sequences so that user space is increased. Extending the sequences results in increasing the number of non-linear feedback shift register cells required to generate 64-bit sequences. The block diagram of 64-bit PCS generator is as shown in Fig.3.

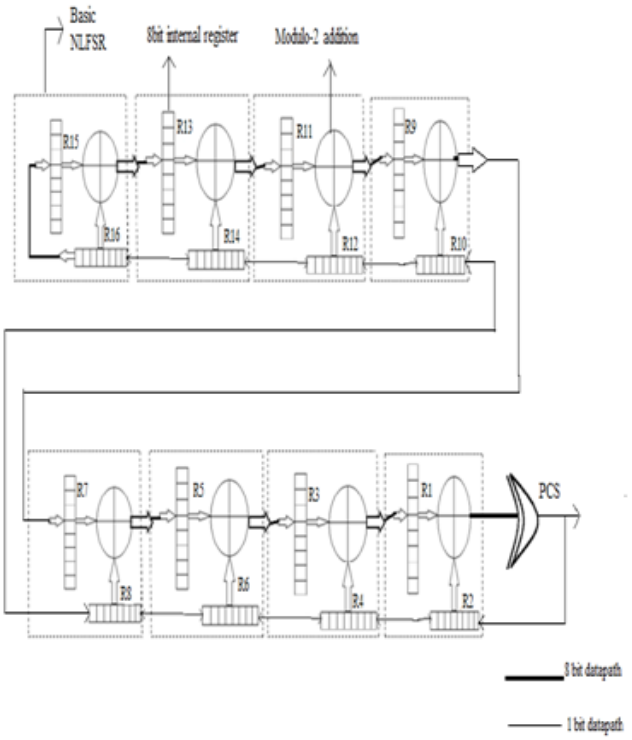

Fig. 3: Block diagram of 64-bit PCS generator

The architecture of 64-bit PCS generator consists of eight NLFSR cells each with two 8-bit programmable registers and XOR function block. All eight NLFSR cells are connected in series. It consists of totally sixteen registers each with 8-bit. Initial conditions are provided to all the sixteen registers.

The operation procedure of PCS generator of 64-bit is as follows: For the first iteration cycle, the contents of the two registers are XORed i.e. modulo-2 addition is performed to obtain 8-bit output Cell out. This output of Cell out is fed as input to the upper register of next NLFSR cell. For the next following iterations, the lower register contents in each NLFSR cell are shifted towards left and thereby changing the contents of two registers in each NLFSR cell. The most significant bit that shifts out of the register is moved to the least significant bit place of the feedback register of the previous cell. Similarly, the shifted bit from the next cell is loaded into the most significant bit place of the lower register i.e. feedback register. The upper register contents are altered by the 8-bit output of the previous cell. The process is repeated till the required 64-bit sequence code is obtained. The PCS generator containing sixteen 8-bit register provide a total of 128 binary memory elements. Therefore, the PCS generator can be viewed as a sequential state machine with at most 264 possible states.

IV. IMPLEMENTATION OF DS-SS SYSTEM

The implementation of DS-SS system is carried out along with Pseudo Chaotic key generator. The block diagram of the implemented DS-SS system with transmitter and receiver is shown in the Fig.4.

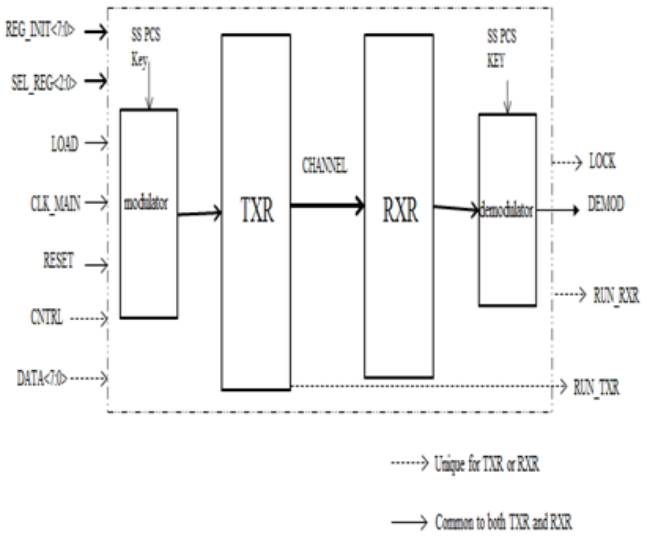

Fig. 4: Block diagram of DS-SS system

In the block diagram, it is clearly shown that the only interconnection between the transmitter and receiver sections is the channel. The message to be transmitted is sent through the medium called as channel which delivers the message to the intended destination. This channel is ideal. Synchronized clock is used in DS-SS implementation.

A. Transmitter

The main function of transmitter is to transmit the modulated data in to the spread spectrum medium effectively by spreading the data over entire available bandwidth using the Pseudo Chaotic Sequences as the key for security. Fig.5shows the block diagram of transmitter in DS-SS system, as in [1].

In this DS-SS system, the data bits spread using PCS sequences. In order to generate PCS sequence, the 8 bit registers R1 to R16 of PCS generator need to be initialized. The signal LOAD is enabled i.e. LOAD=1 to initialize all 16 registers of PCS generator and select the corresponding registers R1 to R16 using 3 pins of SEL_REG. The 8 bit initial values to each of these 16 registers are loaded using 8 pin REG_INIT. An indication to the user is given by READY_OUT pin after loading the initial values to all the 16 registers. Similarly, a signal READY is enabled (READY=1) which signals the control circuit to start its operation. BUSY and DONE signals of control circuit are not enabled initially before loading the initial values to the registers R1 to R16 i.e., the signals are set as BUSY = 1 &DONE= 0. When the signal is set to high i.e. ready = 1, then the signal busy = 0. In order to make the process of tracking and synchronization of receiver easier, the first 8-bits of data are taken as “11111111” and transmitted. Under this condition, a RELOAD signal from the message source end given to the control circuit as an indication that it is ready to send the data. When this happened, in the next clock cycle, the data of 8-bit is sent parallel and it is accumulated in the buffer. The control circuit enables the PCS generator once it receives the 8-bit data by enabling the signal RUN=1. Meantime, the control circuit also allows the multiplier to enable by making ENABLE = 1and points to the buffer that it is busy at this instant by setting the signal BUSY = 1

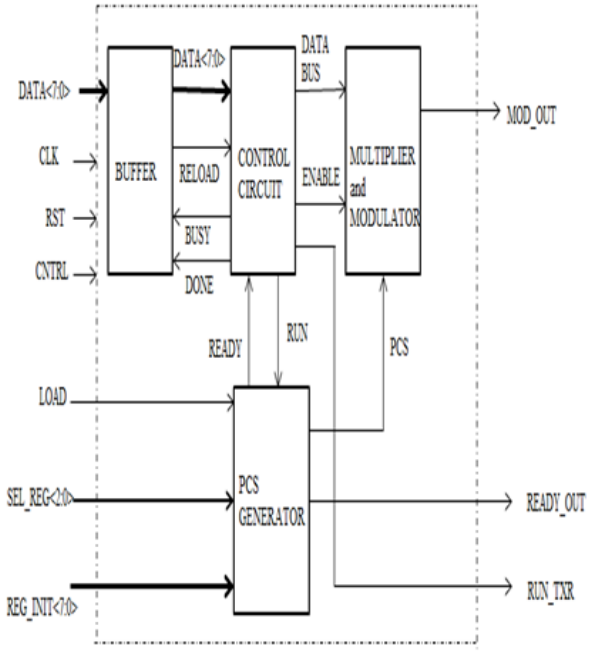

Fig. 5: Block diagram of transmitter[1]

After these steps, the PCS generator starts generating the 64-bits of PCS sequence. The control circuit then starts transferring one bit at a time serially to the multiplier.In the multiplier the bit is multiplied by the 64-bits of generated PCS sequence which results in 64-bits of spread sequence and this obtained sequence is transmitted.After spreading the first data bit by 64-bits of PCS sequence, the multiplier takes the second data bit and is multiplied by the next 64-bits of the PCS sequence and the process repeats until all the data bits are transmitted.For spreading all 8-bits of data, the PCS generator generates a total of 256 bits.After transmission of all the 256 bits with respect to 8-bits of data, the control circuit enables the signal DONE = 1and the signal BUSY = 0. At this instant, the control circuit is ready to receive next frame of 8-bits of data.Thus, the operation of the transmitter repeats in this manner and keeps the gap between the two frames to avoid the interference.

B. Receiver

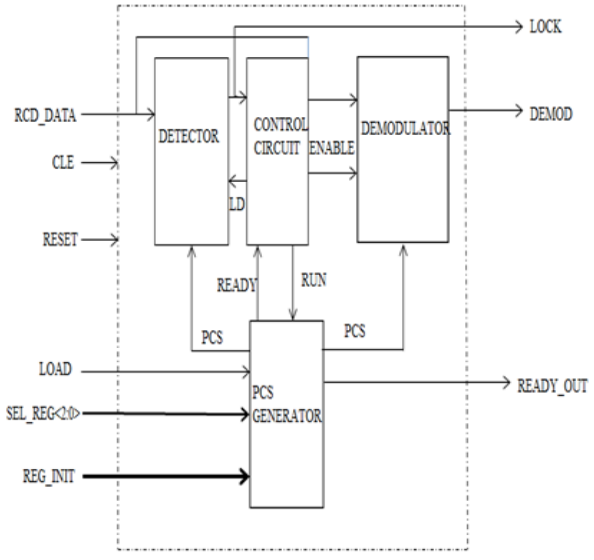

Fig. 6: Block diagram of receiver[1]

Receiver uses the Pseudo Chaotic sequence generator for the generation of the same key of sequences used at transmitter to retrieve the original baseband data. Fig.6 shows the block diagram of receiver section used in the DS-SS system, as in [1].

The operation of DS-SS system receiver is done in three phases. Training, detection and dispreading phase. Before the start of training phase, the same initial values used at transmitter are loaded into all the sixteen registers R1 to R16 used in the PCS generator for initialization process again. PCS generator indicates this to the control circuit by making the READY signal high i.e. READY=1.The control circuit maintains the signal LD=1 and ENABLE=0 and RUN=1 in the training phase of operation.Next, initialization the detector phase is done by loading the training sequences. This is carried out by taking the first 256 bits of the received data into the 8 lower registers of detector where each register is of 32-bit.The control circuit makes the signal LD=0 and RUN=0 during the detection phase.In the detection phase, the 256 bits that are loaded in the 8 lower registers are copied to 8 upper registers of detector where each register is of 32-bit. Now, these loaded values are compared with the pattern of bits that are already present in the 8 lower registers of the detector.The detector passes a signal LOCK=1 to the control circuit after certain threshold value is met. This represents that detection phase is completed and dispreading phase need to start.In accordance with the frame gap duration maintained in the transmitter section, now the control circuit changes the status of signal ENABLE to 1 and RUN=1.Therefore the control of operation is moved to dispreading phase from detector phase.Here the process of multiplication is done on the incoming wideband data stream with Pseudo Chaotic sequences obtained from the generator and thereby the required original narrow band data is recovered at the DEMOD data pin.

V. RESULTS

The results taken for Pseudo Chaotic Sequence generator which is generating 64-bit sequences, modulated output at the transmitter section and demodulated output at the receiver section.

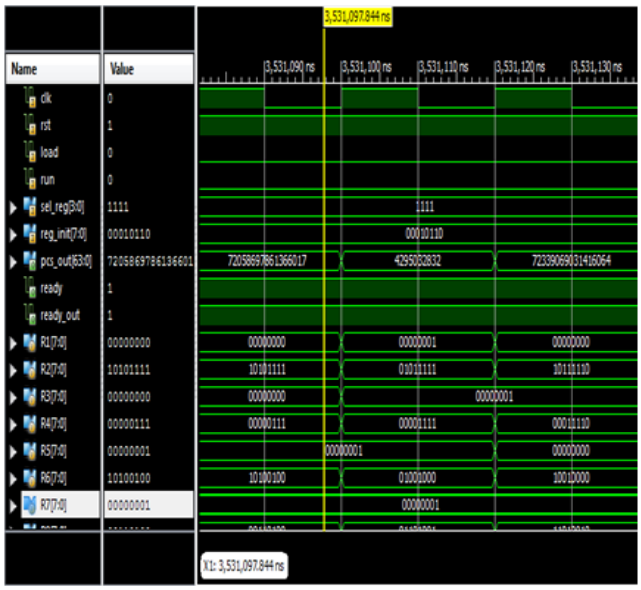

Fig. 7: Output of PCS generator

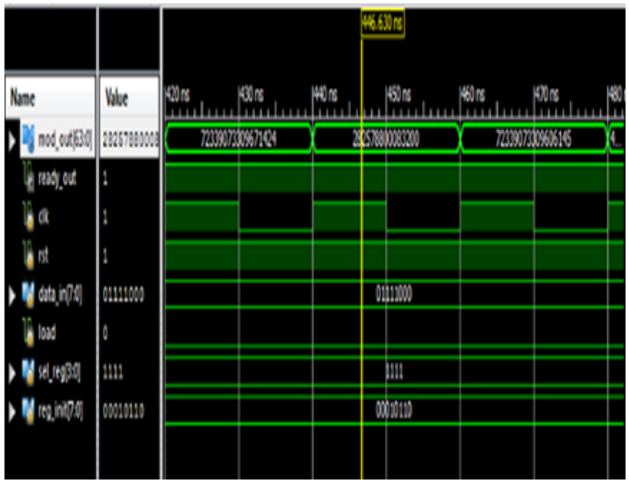

Fig. 8: Output of transmitter

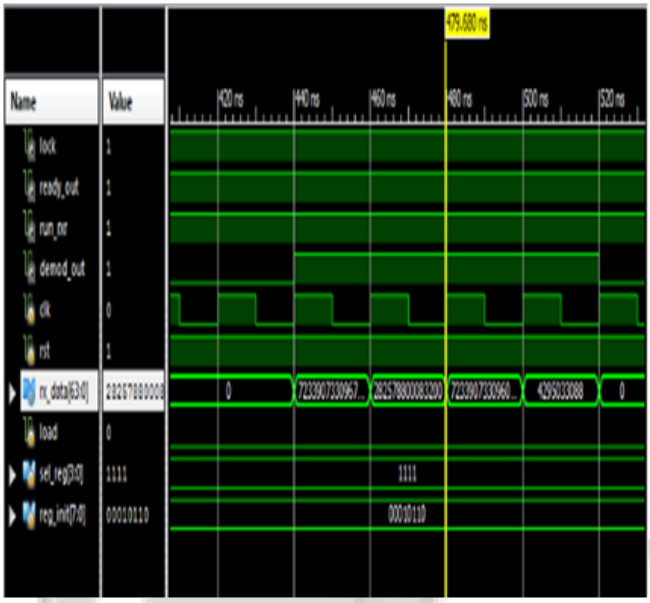

Fig. 9: Output of receiver

The test results include testing the generated Pseudo Chaotic Sequences for auto correlation and Cross correlation. The following table.I show the auto correlation and cross correlation values obtained for the generated Pseudo Chaotic Sequences.

Period N	No. of users K	Auto Correlation	Cross correlation
3	2	17.894	6.693
7	2	3.6832	2.3872
15	2	5.7830	4.3142

Table I: Auto And Cross Correlation Values Of Pcs

From the table it is clear that the auto correlation values obtained are greater than cross correlation values for the generated Pseudo Chaotic Sequences. Cross correlation values obtained are less which means that the Pseudo Chaotic Sequences generated are not identical in each cycle. There is much difference from one sequence pattern generated to another sequence pattern generated in each cycle of iterations.

VI. Conclusion

The Direct Sequence Spread Spectrum system is implemented along with the PCS generator. The design is implemented and simulated in XILINX ISE software tool. The sequence length is increased from 32-bit to 64-bit which made the system performance and user space to increase. The results proved that selecting the initial values randomly generates Pseudo Chaotic Sequences which are comparatively long and have better correlation properties. The tests have proved that Pseudo Chaotic Sequences obtained have very low cross correlation values. Thus these sequences are unpredictable in the system. Therefore, these sequences can be used effectively as the spreading codes in the DS-SS system compared to other conventional PN sequences. Because detection of these sequences is inherently more difficult.

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