Design and Simulation of Digital PWM for Cascaded Multilevel Voltage Source Inverter

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Abstract— Multilevel inverter has a lot of application in the power electronic field, the main application is that the inverter converts a DC to AC, with a lower harmonic distortion, The paper explains the methodology that is the seven level cascaded H-bridge are used to get a lower harmonic distortion in the output Ac voltage with smoother wave by using lower switching frequency, these H-bridge contain less no. of switches so the complexity of the circuit is less. these will be design by using MATALB SIMULIX.

Key words: Cascaded H-bridge multilevel inverter, digital pulse width modulation (DPWM), field programmable gate array (FPGA), Xilinx System Generator

I. INTRODUCTION

A multilevel inverter is a power electronic system that synthesizes a desired output voltage from several levels of dc voltages as inputs. With an increasing number of dc voltage sources, the converter output voltage waveform approaches a nearly sinusoidal waveform while using a fundamental frequency-switching scheme. The primary advantage of multi level inverter is their small output voltage, results in higher output quality, lower harmonic component, better electro magnetic computability, and lower switching losses [1]. While many different multilevel inverter topologies have been proposed, the two most common topologies are the cascaded H-bridge inverter and its derivatives [2], and the Diode-clamped inverter [3]. The main advantage of both topologies is that the rating of the switching devices is highly reduced to the rating of each cell. However, they have the drawback of the required large number of switching devices which equals 2(k-1) where k is the number of levels. This number is quite high and may increase the circuit complexity, and reduce its reliability and efficiency. The various topological structures of the multilevel inverter suggestions must cope with the following points; 1) less number of switching devices, 2) capable of enduring high voltage and high power and 3) lower switching frequency for the switching devices[4-5]

The main advantage of using Cascaded H-bridge is the dc link voltage unbalance between different level does not occur. Due to this advantage Cascaded H-bridge is widely used in the area of stabilizer, high power motor drivers.

In diode clamped inverter the complication is more because of it needs only one dc-bus and the voltage levels are produced by several capacitor in series that divide the dc bus voltage into a set of capacitor voltages. Balancing of the capacitors is very complicated especially at large number of levels.

By using a multilevel inverter the output waveform are in a stepped form; therefore they have reduced harmonic compared to a square wave inverter. The harmonic can be reduced by using a PWM method.

This paper presents how to reduced the harmonic distortion is achieved for a new topology of multilevel inverters using Digital PWM technique. This new topology has the advantage of its reduced number of switching device compared to the conventional cascaded H-bridge. It can be extended to any number of levels. The inverter operation is controlled using switching angles based on PWM with the help of pulse generator. Simulation of higher levels of the proposed inverter topology is carried out using MATLAB. The validity of the proposed topology and the harmonic elimination method are verified experimentally for 7 level inverter.

II. ALGORITHM

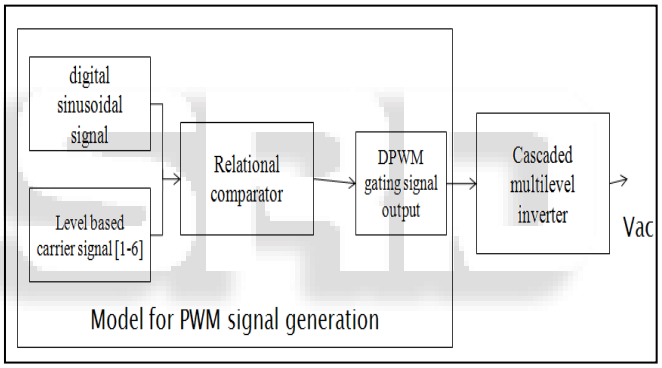

Fig. 1: Model for Cascaded Multilevel Inverter

Fig 1: Shows the technique used to generate the output waveform with the reduced harmonic reduction by using a Digital PWM is given to the input for the Cascaded H-bridge 7-level inverter. The DPWM signal is generated by using a comparison of different carrier signals with the sinusoidal signal. The saw tooth wave as a carrier signal are used and generated by up counter devices in Xilinx system generator toolbox of the MATLAB. The first counter starts from 0V to 1V of saw tooth wave carrier signal, and second counter start from 1V to 2V of the saw tooth wave carrier signal amplitude is kept with a constant amplitude and frequency of 1kHz. The reference sinusoidal wave signal of 6V amplitude and 50Hz frequency is approximated by a stepped sinusoidal generated using a 5-bit up counter with 14-bit memory device. The generated DPWM signals are given as input to the Cascaded 7-level inverter.

III. MULTILEVEL INVERTER NEW TOPOLOGY

In order to reduce the overall number of switching devices in conventional multilevel inverter topologies, a new topology has been proposed. The circuit configuration of the new &-level inverter is shown in fig 2. It has four main switches in H-bridge configuration Q1, Q2, Q3, Q4, and

four auxiliary switches Q5, Q6, Q7, Q8. The corresponding output voltage waveform, load current, and gating signal are shown in Fig 3,

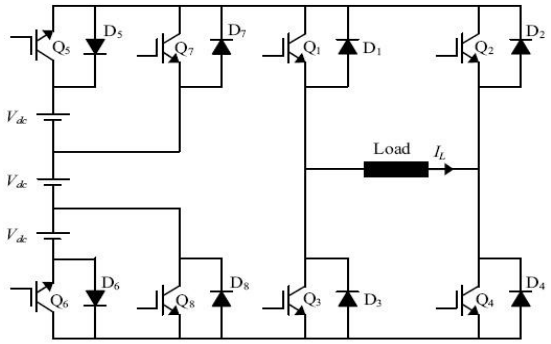

Fig. 2: The 7-Level Inverter of the New Topology

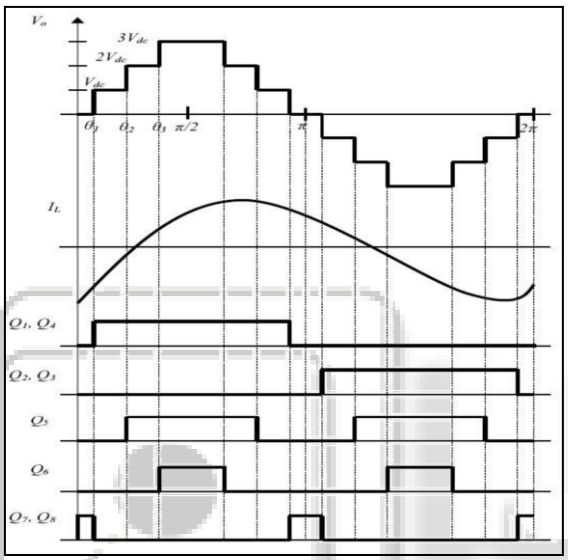

Fig. 3: Waveforms of the Proposed 7-Level Inverter

IV. SIMULATION RESULTS

The feasibility of the proposed approach is verified using computer simulations. A model of the seven-level inverter is constructed in MATLAB-Simulink software. A new strategy with reduced number of switches is employed. For cascaded H bridge 7 level inverter requires 12 switches to get seven level output voltage and with the proposed topology requires 8 switches. The new topology has the advantage of its reduced number of devices compared to conventional cascaded H-bridge multilevel inverter, and can be extended to any number of levels The schematic of the cascaded H bridge seven level inverter and proposed new seven level topology built in MATLAB-Simulink is illustrated in Fig. 4 and Fig. 5 respectively.

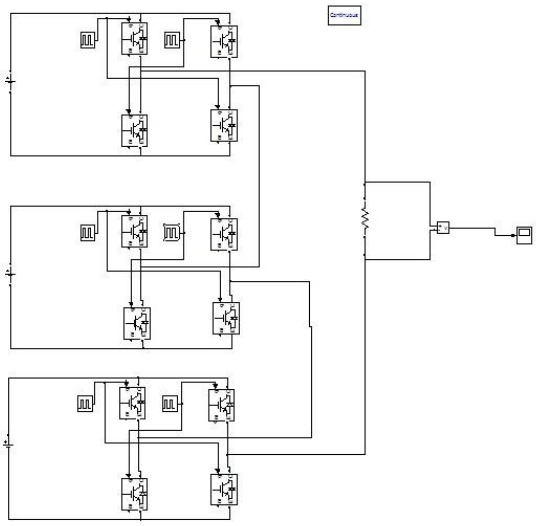

Fig. 4: Schematic of Conventional Seven Level Inverter

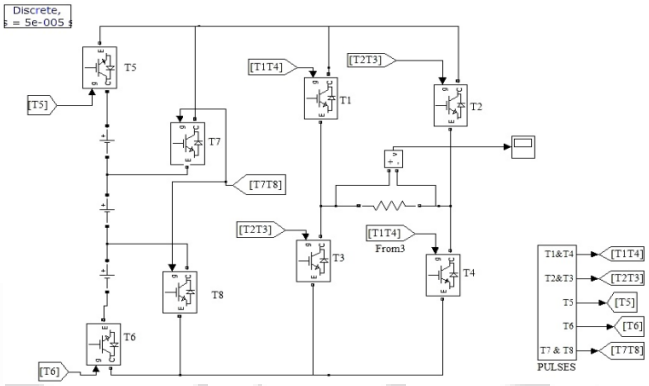

Fig. 5: Schematic of conventional Seven Level Inverter

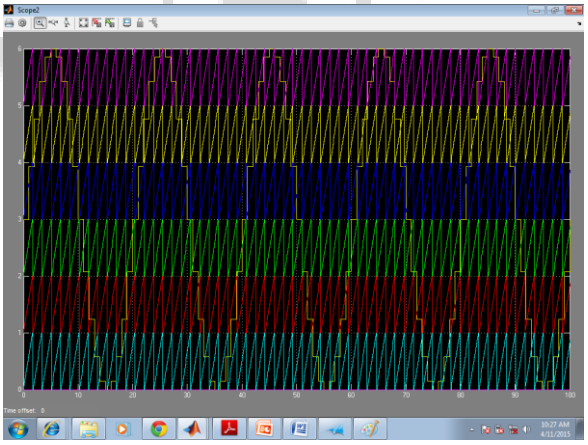

Fig. 6: Six Different Levels Of Saw Tooth Carrier Signal Compared With Digital Sinusoidal Counter Based Signal.

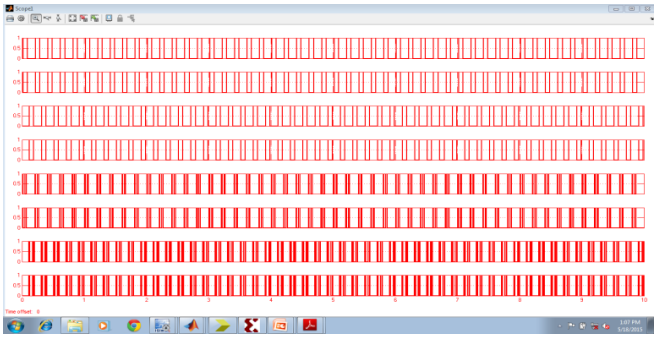

Fig. 7: Switching Pattern of Single Phase Seven Level Inverter Topology

Fig. 8: DPWM Signal In Xilinx Syatem Generator

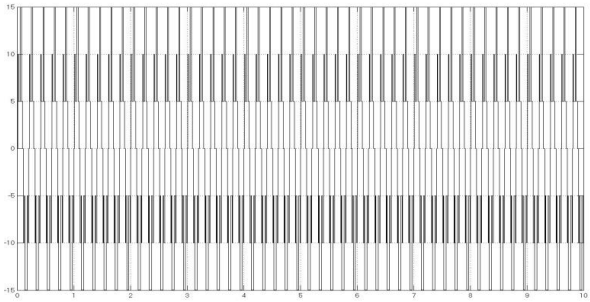

Fig. 9: Output Voltage for Single Phase Seven Level Inverter

V. CONCLUSION

A new family of multilevel inverters has been presented and built in MATLAB-Simulink. It has the advantage of its reduced number of switching switches compared to conventional similar inverters. However, the high rating of its four main switches limits its usage to the medium voltage range. The modes of operation and switching strategy of the new topology are presented. A PWM algorithm is applied with the help of pulse generator and based on the theory of resultant has been applied for harmonic elimination of the new topology. Since the solution algorithm is based on solving polynomial equations, it has the advantage of finding all existed solutions, where the solution produces the lowest THD is selected. Other PWM methods and techniques are also expected to be successively applied to the proposed topology. The simulation results show that the algorithm can be effectively used to eliminate specific higher order harmonics of the new topology and results in a dramatic decrease in the output voltage THD.

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