Design of Polar List Decoder using 2-Bit SC Decoding Algorithm

V Priya 1 M Parimaladevi 2

1 Master of Engineering 2 Assistant Professor
1,2 Department of Electronics and Communication Engineering
1,2 Velalar College of Engineering and Technology, Erode

Abstract—The number of decoding architecture techniques are introduced for wireless communication channel. Such architectural techniques aim to improve the latency, area and complexity of various methods. This paper aims to get solution for FPGA based list decoder architecture, achieving the latency, area and throughupt of the system. In this paper, 2bit Successive Cancellation (SC) decoding algorithm is used in polar list decoder architecture. Also, the usage of CRC in list decoder increases the throughput. The architecture is implemented in Xilinx Spartan 3E FPGA device. The result shows that the latency is reduced up to 64% compared to conventional SC decoder. The proposed design achieves area and delay of 88% & 17.3% than conventional SC decoder.

Key words: Polar Codes, Successive Cancellation, Polar List Decoder, 2-Bit SC Decoding Algorithm

I. INTRODUCTION

Polar codes are introduced by Erdal in (1), are a new class of error correcting codes due to their capacity achieving property. It is the first code with explicit construction to provably achieve the channel capacity for symmetric binary-input discrete memory less channels (B-DMC). The significant investigation has been directed toward code constructions and improvement of error correction performance of polar codes with short and moderate lengths (2)-(4). The error correction performance of SC algorithm is worse than that of Turbo codes and Low-density parity check codes. However, for polar decoder design, further research is still required. For successive cancellation algorithm [5], leads to a very long decoding latency and the complexity of the SC decoder is O (NlogN), where N=2^n is the code length. In (6), an FPGA implementation of belief propagation (BP) was described. The BP decoder has particular advantages in parallel design but not striking for practical applications due to their large processing elements. In order to guarantee good performance, polar codes length N needs to be greater than 2^10.

For future real-time applications, the designs of low-latency SC decoders are required. A polar list decoder is proposed to perform minimum clock cycles than the SC algorithm. This paper presents two-bit decision approaches that can reduce the latency of conventional SC decoders. First, reformulated component of list decoder using 2-bit SC decoding algorithm, which can perform intermediate decoding of 2-bits simultaneously. Then by, apply the reformulated component of list decoder in polar list decoder architecture, is presented to reduce the overall latency from 14 clock cycles to 5 clock cycles. Based on both algorithm and architectural enhancements, our decoder architecture achieves better error performance and high area efficiency compared with other decoder architecture in (7).

In (8), the list decoder architecture was presented to contribute single bit in processing unit array, which has leads to high latency and area overhead. In this paper efficient processing unit (PU) is proposed. For the proposed polar list decoder architecture, a 2-bit reformulated decoding algorithm is proposed to determine the minimum size of each input message for each PU so that there is no message overflow. Using the algorithm for each PU, the overall latency and area of PUs is reduced.

The remainder of this brief is organized as follows. Section 2 presents a related work of the SC algorithm and 2-bit SC algorithm. In Section 3, the proposed work for the polar list decoder Section 4 presents the experimental results and parameter comparison of latency area. The final section concludes this brief.

II. RELATED WORK

This paper is extension of work initiated in (1). Where the 2-bit reformulated SC algorithm is reduce the latency over conventional SC algorithm. In that last stage is reformulated through p node which requires minimum processing elements. The remainder of this paper is follows:

A. Polar Encoder

The (n, k) polar code contains k information bits and (n-k) frozen bits. These (n-k) frozen bits are fixed at “bad” position and information bits are fixed at “good” position. The information bit is also called as non-frozen bit. The polar encoder needs 8 input information bits and it transmitted to convert a code word. Each input is depends on one another (1). And the converted code word passed through three stages of polar encoder. The input of the polar encoder is to construct n-bit source data vector as u=(u1, u2,……u_k). Where u_i= c_i, if i= free_i; or u_i= 0, if i= frozen_i. Here c_i indicates original k-bit information message. After obtaining code word u next to computes the code word x=(x_1, x_2,……x_n) by the generator matrix G. The encoded output is given by,

\[ X = u \cdot G \]  

(1)

The generator matrix is constructed using the n th kronecker power of the matrix F=[ \begin{bmatrix} 1 & 0 \\ 1 & 1 \end{bmatrix} ]. For example n=3, F=[ \begin{bmatrix} 1 & 0 \\ 1 & 1 \end{bmatrix} ].

The equivalent implementation of polar encoder with n=8 is shown in Figure 1. For the reliability of transmission, the information bits and frozen bits are fixed at “good” and “bad” positions. Finally, the encoded output is transmitted through the channel.
B. Existing Conventional SC Decoder

The original information bits are retained in the receiver part by decoding the code word. But the receiver end corrupted by the transmission noise, the received code word will no longer be x but change to y= (y1, y2,……yN). With the recursive computation procedure the SC algorithm can use the likelihood ratio (LRs) of y to estimate the decoder. The SC algorithm proposed by Arikan is shown in algorithm 1. The estimated output is represented by u= (u1, u2,......uN). The decoded output information obtained back is as follows initially u0, and then comes u1 and finally uN-1. The output of each decoded bit ûi is obtained by the following decision function h (.) (1) and ûN is the previously decoded bits.

\[ û_i = h(LR[y, û_{i-1}]) \]  

where h[LR[y, û_{i-1}]]=1 if i is not frozen position and h[LR[y, û_{i-1}]]=0 if i is frozen position.

Algorithm 1: Successive Cancellation (SC)

For i=0,1,2,……N-1 do
If i € k then
\[ û_i = u_i \] //frozen bits
else
\[ û_i = 0 \] //non-frozen bits
return ûN

The likelihood ratio of the conventional SC decoder it uses two functions f and g with three stages depending on each other. And these two functions f and g are employed to calculate LR[y, û_{i-1}]. Here LR[y, û_{i-1}] in stage-3 is calculated from the stage-2, and the stage-2 needs the information message from stage-1. Since these intermediate propagating messages are also LR values. The f and g functions are defined by,

\[ f(a, b) = 1 + ab/(a + b) \]  

\[ g(a, b, u_{sum}) = a^{1-2u_{sum}b} \]  

In equation (4), u_{sum} is the modulo-2 sum of partial previous decoded bits. And the term u_{sum} represents the “successive” operation in the SC algorithm. To clearly illustrate this phenomenon, the conventional SC decoder is shown in Figure 2.

From this Figure 2. The decision of current bit strongly depends on the previous decoded bit; therefore the decoded bits can only be computed successfully. From that decoded output, the decision unit decides correct or not, by denoting it as either 0 or 1. By using the SC algorithm in polar decoder, increase the latency and complexity.

C. Existing 2-bit SC Decoder

The 2-bit SC algorithm is shown in algorithm 2. In this 2-bit SC decoder last stage is reformulated through p node. Since the p node it performs the same output of conventional SC decoder instead 2-bits to be decoded in the same clock cycle and the remaining operation is same as conventional SC decoder. The 2-bit SC decoder is shown in Fig. 3. From this Figure 3. p node it performs the operation of U2i-1 and U2i in the same cycles. The process of p node is given by,

\[ U2i - 1 = L1 \ XOR \ L2; \]  

\[ U2i = L1 \ XOR \ U1; \]  

From this above equation 2-bits are decoded in the same clock cycles. Therefore, the overall latency is reduced from the conventional SC decoder. And also clock cycles get reduced from 14 clock cycles to 10 clock cycles.

Algorithm 2: 2-bit Successive Cancellation (SC) Decoding Input: Log - Likelihood ratios LLR(c) and LLR(d) from stage- m-1.

Judge u2i-1 and u2i are frozen bits or not.

(1) Case 1: None of u2i-1 or u2i is a frozen bit.
Find the largest element among \{LLR(c) + LLR(d), 0, LLR(c), LLR(d)\}.
If the largest element is LLR(c) + LLR(d): u2i-1 = 0, u2i = 0.
If the largest element is 0: u2i-1 = 0, u2i = 1.
If the largest element is LLR(d): u2i-1 = 1, u2i = 0.
If the largest element is LLR(c): u2i-1 = 1, u2i = 1.

(2) Case 2: Both u2i-1 and u2i are frozen bits u2i-1 = 0, u2i = 0.

(3) Case 3: only u2i-1 is frozen bit,
\[ u_{2i-1} = 0, \]
\[ u_{2i} = 0, \] if LLR(c) + LLR(d) ≥ 0
\[ 1, \] if LLR(c) + LLR(d) < 0

Case 4: only u2i is frozen bit,
\[ u_{2i} = 0, \]
\[ u_{2i-1} = 0, \] if sign(LLR(c))sign(LLR(d)) ≥ 0
\[ 1, \] if sign(LLR(c))sign(LLR(d)) < 0

Output: u_{2i-1}, u_{2i}
III. PROPOSED WORK

A. Proposed List Decoder

In proposed method 2-bit SC decoder algorithm is implemented in list decoder architecture. This reduces the latency and area. The new form of decoder is known as the polar list decoder. The component of list decoder is shown in Figure 4, and the overall architecture is shown in Figure 5. This 2-bit SC decoding algorithm in polar list decoder performs intermediate decoding of 2-bits simultaneously.

The process of list decoder performs initially the input can be loaded from the channel; it can be likelihood values of either 0 or 1. After the value passes through the different stages and last stage is reformulated through 2-bit SC decoder replaces the original stage-m with two units, referred as metric computation unit (MCU) and zero-forcing unit (ZFU) respectively. The metric computation unit calculates the different combinations of input with the use of the messages a(0),a(1),b(0) and b(1) output from the stage(m-1). From the output of metric computation unit performs intermediate two bits can be loaded at the same clock cycles, and also reduce the overall latency from the conventional SC decoder.

The output of metric computation unit passed through the zero-forcing unit. From that it avoids some unqualified paths. The value of U_{2,1} and U_{2,0} do not only depend on the corresponding path matrices but also whether they are frozen bits or not. Finally M(00),M(01),M(10) and M(11) are the output of component list decoder. The component list decoder is implemented in list decoder architecture with the help of processing unit array, the architecture performs different functions:

1) Message Memory Architecture (MMA): It performs internal computations and storing channel messages.

2) Processing Unit Array (PUA): These processing unit performs metric computation unit and zero forcing unit i.e., f, g, p nodes.

3) Partial Sum Network (PSU): To speed up the partial sum network.

4) Cyclic Redundancy Check (CRC): The CRC to find out the correct output list decoder.

IV. RESULT ANALYSIS

In signal processing, Polar code technique is implemented where a higher channel capacity can be achieved. By using this, the utilization rate of channel will be attained and the complexity of the Processing Elements is reduced by decoding method while transmitting the information bits from sender to receiver.

Generally, error detection and correction can be achieved by adding a redundancy bits to the message, where receiver can check the reliability of the data that has been transmitted without any error. In systematic method, by using some deterministic algorithm the transmitter sends the original data along with check bits. If the values are getting mismatched then at some point in the transmission side error has occurred. Unlike in non-systematic method, the message will be encoded. Communication channel plays a major role for good error control performance. Initially streaming data’s are loaded into the polar encoder. The encoded data’s are forwarded to receive via communication channel. At receiver, data’s are again loaded into the processing elements and decoding using SC and 2-bit SC algorithm. The Figure 7, Figure 8 and Figure 9 show the design summary of conventional SC decoder, 2-bit SC decoder and polar list decoder. The output of the conventional SC decoder and 2-bit SC decoder are shown in Figure 10 and Figure 11. By comparing these decoders the 2-bit SC decoder reduce the latency over conventional SC decoder. By implementing 2-bit SC algorithm in list decoder, it greatly reduces the latency and area. The RTL view of the polar list decoder is shown in Figure 6.

![Fig. 3: 2-bit SC decoder](image1)

![Fig. 4: Reformulated component of list decoder](image2)

![Fig. 5: Architecture of Polar List Decoder](image3)

![Fig. 6: RTL View of Reformulated Component of List Decoder](image4)
By applying likelihood values from the channel to the list decoder performs intermediate decoding of 2-bits simultaneously. From these 2-bits to be decoded instead of same clock cycles, which can reduce the clock cycles of 5. The output of the polar list decoder is shown in Figure 12. The proposed polar list decoder architecture shown in the previous section is implemented and resulted from using Verilog and simulated in Xilinx ISE 9.2i. Table 1 shows the implementation result analysis of existing and proposed decoders. Implementing the decoders the polar list decoder achieves the better latency and area than the SC decoder.

![Fig. 7: Design Summary of Conventional SC Decoder](image)

![Fig. 8: Design Summary Of 2-Bit SC Decoder](image)

![Fig. 9: Design Summary of 2-Bit SC Decoder](image)

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Existing Conventional SC decoder</th>
<th>Existing 2-Bit SC decoder</th>
<th>Proposed Polar list decoder</th>
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<tbody>
<tr>
<td>Combinational Path Delay</td>
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<td>26.450</td>
<td>25.206</td>
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<tr>
<td>Latency(Clock cycles)</td>
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<td>10cycles</td>
<td>5cycles</td>
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<td>LUT</td>
<td>1408</td>
<td>704</td>
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<tr>
<td>Gate Count</td>
<td>9996</td>
<td>5004</td>
<td>1194</td>
</tr>
</tbody>
</table>

Table 1: Implementation Results of Latency and Clock Cycles Analysis

V. CONCLUSION

Latency is an important factor in VLSI because it reduces the efficiency of the system. In order to increase the efficiency, latency must be reduced. The 2-Bit SC decoder achieves the lower latency due to its series connected p node which offers 2-bits that are decoded simultaneously instead of single bit. Our proposed system avoids processing elements at last stage by replacing simple elements. This reduces the overall latency from of 64% from the conventional SC algorithm and also 88% of area is minimized. Simulations are carried out over various input data bits and got the decoded output is obtained from the original source data vector using Xilinx Spartan 3E FPGA kit.

REFERENCE


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