Low Power Reduction Technique in VLSI

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Abstract— Power and performance have become the predominant concern for chip designers in deep submicron technology due to the continuous scale down of the device for satisfying the Moore's law which state that the number of transistor per chip will be double in every eighteen month. When the channel length shrinks, the absolute value of threshold voltage become smaller due to the reduced controllability of the gate over the channel depletion region by increasing charge sharing from source/drain which results in the increase in sub threshold leakage current exponentially, so the static power dissipation increased. In the deep submicron technology CMOS power dissipation plays a vital rule. Various comprehensive studies on leakage power minimization technique have been studied in this paper focusing on circuit performance parameter.

Key words: low power, sub-threshold, Delay

I. INTRODUCTION

As the semiconductor technology advanced day by day the density of transistors in integrated circuit is increasing day by day. Power dissipation consists of leakage power and dynamic power. Dynamic power includes the switching power and short circuit power. Switching power is increase when the transistors are in active mode.[1] And short circuit power is occur when both pull up and pull down transistor are in turn on during a short period of time. For the sub micron technology leakage power is very small compared to the dynamic power but as the device is continuously scale down the leakage power is dominant factor. As dynamic power is proportional to the square of the supply voltage, so in deep submicron technology, the threshold voltage and supply voltage for the MOS transistors are greatly reduced, static power is the power dissipation due to the leakage currents which flows through a transistor when no it is in the steady state. Leakage power is depends on gate length and oxide thickness and it varies exponentially with threshold voltage and supply voltage and other parameter.[2][3] So reduction of threshold voltage and supply voltages for MOS transistors which helps to reduce dynamic power dissipation which become a disadvantage for leakage power. The sub threshold leakage current increases exponentially, thereby static power dissipation. The main source of leakage power in CMOS inverter is Reverse-biased junction leakage current; Gate induced drain leakage, Gate direct-tunneling leakage and Sub threshold (weak inversion) leakage current.

II. SUB THRESHOLD LEAKAGE CURRENT

Sub threshold current is the current of minority electron flowing by means of diffusion p type substrate from source to drain.[4] Exponential dependence of the minority carrier concentration on the gate and drain voltages leads to an exponential I(V) characteristics

$$I_{sub} = \mu_n C_{ox} \frac{w_n}{L_n} V_t^{\,2} \exp\left(\frac{V_{gs}-V_{th}}{nV_{th}}\right)[(1-\exp\left(-\frac{V_{ds}}{V_t}\right)] \quad \text{…….. (1)}$$

Sub threshold off current for $V_{gs} = 0, V_{ds} > V_T$

$$I_{subth} = \mu_n C_{ox} \frac{w_n}{L_n} V_t^{\,2} \exp(-\frac{V_{th}}{nV_{th}})$$

So the dependence of the sub threshold current on the transistor parameter given below:

- Increase exponentially when threshold voltage is reduce
- Increase with decreasing the channel length
  - Direct dependence
  - Short channel effect
  - Drain induced barrier lowering effect.
- Increasing with temperature

III. LOW POWER REDUCTION TECHNIQUE

Based on modes of operation of the system there are several leakage power technique. Two modes are 1) active mode 2) idle mode. Most of the technique concentrates power reduction by shutting down the power supply voltage on standby mode.

A. Dual threshold in CMOS

This technique uses two threshold voltage, high threshold voltage and low threshold voltage. High threshold voltage uses on non critical path of transistor to reduce leakage power and low threshold voltage used on critical path to maintain the circuit performance.[5] When transistor is off, the dynamic threshold CMOS the gate and body of the transistor are tied together to reduce the leakage power.

B. Variable threshold in CMOS

This technique modifying the threshold voltage dynamically in active mode which is known as standby power reduction. In this technique the threshold voltage is raised in standby mode by connecting the substrate voltage either higher than(PMOS) or lower than (NMOS) ground, but the limitation of this technique is that it is required an additional power supply which is not applicable for many commercial designs.

C. Multi threshold CMOS

In this technique, a SLEEP transistor is formed by inserting a high threshold device in series with low threshold devices in between the power supply voltage and the ground.(fig 1). This SLEEP transistor is turned on during active mode as the normal operation of the transistor is not getting affected because of the path in between the power supply and the ground. The SLEEP transistors are turned off in standby mode so shutting down the power supply to this circuit by creating a virtual power supply and ground rails. This teqnique is very popular and knows as SLEEP TRANSISTOR.

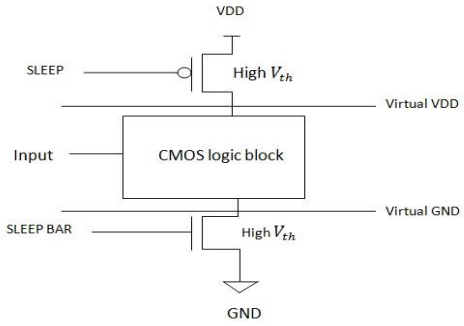

Fig. 1: structure of Multi Threshold CMOS

D. Super cutoff CMOS

In technique is similar to the multi threshold CMOS technique. In this technique the Vgs of the SLEEP transistor is over driven and under driven in the standby mode. The interesting features of the super cutoff CMOS is that the SLEEP transistor have low threshold voltage which ensures the high speed operation of the logic circuits.(fig 2)

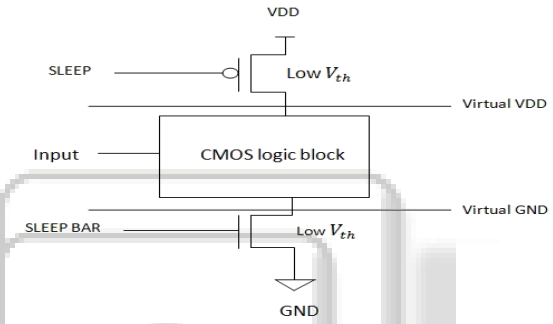

Fig. 2: structure of super cutoff CMOS

E. Transistor stacking effect

Transistor stacking is a useful technique which is used in active mode for the leakage power reduction. When two or more series transistor is turned off then the leakage current is decreases and it is called stacking effect or self reverse biased effect. The output of the gate is high when it is in the standby mode. This means that the pull down network is off. Therefore putting a transistor in series with the pull down network and keeping it off in the standby mode will not change the value of the output. However it will increase the resistance between the power supply and ground, and the leakage of the logic gate is reduced. Here force stacking is implemented where a single transistor of width "W" is replaced by of two transistor of width W/2.(fig 3). Which results the two transistors is turning off at the same time, so the leakage current is reduced.

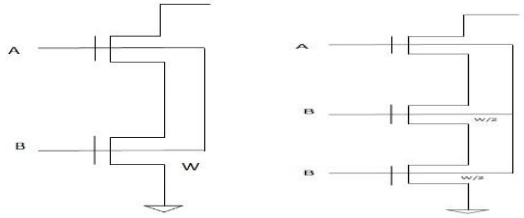

Fig. 3: Forced stacking

F. Sleepy stack

This approach is same as the transistor stacking approach shown in fig (4). In this technique force stacking is the first implementation and then inserting of sleep transistor parallel to one of the stack transistors. Two parallel transistors are on during the active mode; therefore the active resistance of the path is reduced which results in less propagation delay. During the standby mode the sleep transistor is turned off and the stack transistor reduces the leakage power.

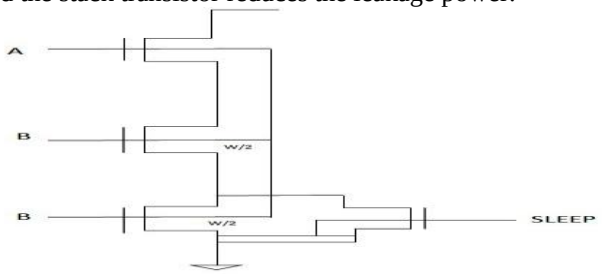

Fig. 4: Sleepy stack

G. Sleepy keeper

In this scheme an additional NMOS transistor is placed in parallel with pull-up transistor connecting VDD to the pull up network. During the sleep mode as the sleep transistor is off, the NMOS transistor is the only source of VDD to the pull up network. Similarly an additional single PMOS transistor is placed parallel with pull-down sleep transistor which becomes the only source of GND to the pull down network. In sleep mode the PMOS transistor connected to ground to maintain output value equal to "0"and the NMOS transistor connected to VDD to maintain the output value "1" respectively (shown in fig:5)

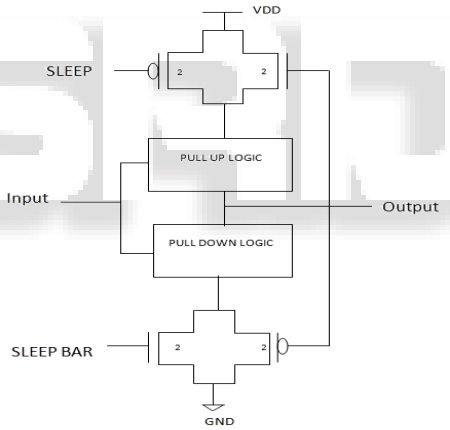

Fig. 5: Sleepy keepers

H. Input vector control

To obtain the minimum leakage vector (MLV) an algorithm is given by [14]. The Leakage current of INVERTER 2 input NAND and 3- input NAND for different inputs [16] are given in the tables I, II and III respectively.

Input	Leakage(nA)
0	100.1
1	226.4

Table I: leakage current of inverter

Input	Leakage(nA)
00	37.84
01	100.10
10	95.18
11	454.5

Table II: Leakage current of 2-input NAND

Input	**Leakage(nA)**
000	22.84
001	37.84

010	37.84
011	100.10
100	37.02
101	95.16
110	94.88
111	852.4

Table III: leakage current of 3 input NAND

I. Leakage control transistor

In this technique the leakage control transistor i.e. PMOS and NMOS transistor is placed in between the pull-up and pull-down network within the logic circuit shown in fig(6). The transistors are connected in such a way that one of the transistors is always cutoff voltage for any input combinations. This increases the resistance path from power supply to ground which leading to significant reduction of leakage current. This leakage control transistor is effectively works in both active mode and standby mode.

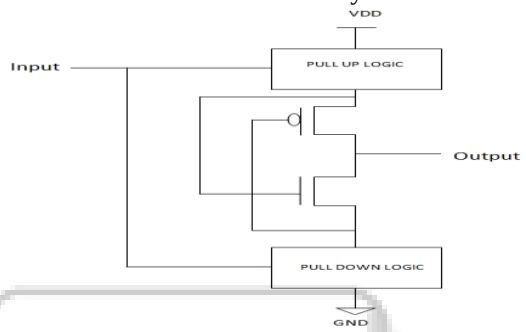

Fig. 6: leakage control transistor

IV. ANALYSIS OF LEAKAGE CURRENT REDUCTION TECHNIQUE

The circuit performance parameter such as the power, delay and power delay product has been analyzed in this section (shown in table: IV). The full adder with sleepy keeper is shown in fig (7). Percentage of power saving, delay and area of the 2- input NAND circuit shown in table: V.

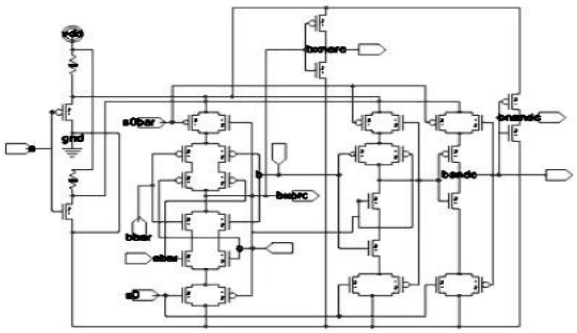

Fig. 7: full adder with sleepy keeper

Technique	**Leakage power(μW)**	**Dynamic power(μW)**	**Delay (ps)**	PDP_{static}
Basic case	301.1	7.23	77.8	23.42
Forced stacking	206.9	7.32	79.71	16.491
Input vector control	87.02	7.32	79.7	6.935
Sleepy stack	211.3	7.45	79.43	16.783
Power gating with stacking	209	7.14	90.14	18.839
Power gating with PMOS only	33.55	7.45	81.421	2.731
Power gating with NMOS only	26.14	6.93	84.37	2.205
Power gating with PMOS and NMOS	4.58	7.15	88.39	0.4048
Super cut CMOS – PMOS only	28.25	7.43	81.36	2.298
Super cut CMOS – NMOS only	25.62	6.98	83.65	2.143
Super cut CMOS – PMOS & NMOS	3.16	7.11	88.04	0.2782

Table IV: power dissipation, area and delay of full adder

Technique	Power saving	Delay	Area
Multi threshold CMOS	10%	4.6- 8.3%	2%
Variable multi threshold CMOS	50%	25%	1%
Dual threshold CMOS	98%	44%	0%
Leakage control transistor	30.20%	18.79%	

Table IV: power dissipation, area and delay of 2 input NAND

Technique	**Advantage**	**Disadvantage**
Forced stacking	Easy to implement ,leakage current reduction	Propagation delay increases.
Sleepy stack	Less delay compared to forced stacking	Sleep transistors need control circuit
Input vector control	High power saving compared to forced stacking	Control circuit is very complex,
Power gating with stacking	More leakage savings in both operating modes	Delay increases,
Power gating PMOS &NMOS	Large power savings, most preferred method.	Control circuit is needed.
Super cutoff CMOS	Best power savings, Easy to fabricate	Control circuit
Leakage control transistor	Control circuit is not required, Best	Delay increases.

Table IV: Advantage and disadvantage of leakage current technique

V. CONCLUSION

The leakage power reduction plays a vital rule in low power VLSI circuit design. To fulfill the Moore's law the device is continues scaling down which lead s some significant effect. The present study provides a choice for leakage power reduction technique for a specific application by a VLSI circuit designer based on sequential analytical approach. It can be concluded that the importance performance parameter s such as leakage power, dynamic power, propagation delay, PDP are strongly inter related. And it can be found that the leakage control transistor technique is the more effective in both active mode and standby mode of operation and it is suitable for faster circuit operation. If consider propagation delay is the main criteria then super cutoff CMOS is suitable for standby mode operation and force stacking is suitable for active mode of operation.

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