Modern development environment for implementing ladder logic of Micro-PLC on FPGA

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Abstract— Inside the PLC base on microprocessor which is executing ladder diagram sequential. But the performance of PLC is limited by the length of program and operation speed of the microprocessor. PLC doesn’t executing parallel rung of ladder diagram concurrently. Ladder Diagram is a form of graphical language type PLC programming that represents the schematics of electrical relay circuit diagram. A new technology such as Field Programmable Gate Array (FPGA) for industrial process control applications. To enhance the performance of traditional PLC, an approach to design and develop a new micro-PLC based on FPGA. FPGA has provided optimal performance, parallel execution mechanism and hardware structure. Therefore, to convert ladder diagram into VHDL program for increase the performance of PLC. Therefore, implement GUI (Graphical User Interface) tool base on Visual Studio 2010 platform, for ladder diagram entry and then automatic convert ladder diagram to VHDL code. Synthesis and simulate generated VHDL code for micro-PLC base on FPGA. The conversion process of ladder diagram to VHDL is verify and demonstrates by simple example.

Key words: PLC, FPGA, Ladder Diagram, VHDL.

I. INTRODUCTION

Programmable Logic Controller (PLC) is one type of programmable controllers, which is used in industrial applications. PLC based on microprocessors which executing program sequential and cyclic way. PLC is a sequential processor which cannot execute parallel rungs of ladder diagram concurrently. But the performance of traditional PLC will be restricted by the operation speed of the microprocessor. It is difficult to adapt to the requirements of high-speed control in modern industry. Therefore, find out a way to realize high-speed control becomes more and more important.

To increase the performance of PLC an approach to design and develop a new hardware controller design based on Field Programmable Gate Array (FPGA). FPGA offer high-speed parallel processing, and reconfigurable hardware structure, low implementation cost, high flexibility and greatly improved performance. FPGA can greatly improve the execution speed of control logic and this is an important way to solve the current problems of PLC. So, that to convert ladder diagram program of PLC to Very High Speed Integrated Circuit Hardware Description Language (VHDL) for new hardware controller design based on FPGA. Therefore, implement GUI (Graphical User Interface) tool base on Visual Studio 2010 platform, for ladder diagram entry and then automatic convert ladder diagram to VHDL code. Synthesis and simulate generated VHDL code for micro-PLC base on FPGA. The conversion process of ladder diagram to VHDL is verify and demonstrates by simple example.

II. PROGRAMMABLE LOGIC CONTROLLERS (PLC)

PLC consists of a central processor unit (CPU), input modules, output modules, power supply, user programming interface port as shown in Fig.1. [1], [4], [6]

![Fig. 1: Block Diagram of PLC](image)

A. Ladder diagram (ld)

Ladder Diagram is a form of graphical language type PLC programming that represents the schematics of electrical relay circuit diagram. As the name of Ladder Logic diagram implies, it basically resembles the ladders with horizontal rungs and vertical rails. Besides that, it consists of basic elements which are power source, inputs such as switch, output and interconnecting wires as shown in the Fig. 2. [6], [8]

![Fig. 2: Simple ladder diagram](image)
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III. MODERN DEVELOPMENT ENVIRONMENT

The modern development environment is show in fig. 4. Block-A, GUI is developed base on visual studio 2010 for ladder diagram editor. It used to create, edit new ladder diagram of PLC. Block-B is heart of development environment. It is convert ladder diagram into VHDL code and automatic to generate the VHDL code for this ladder diagram. In Block-C, to optimize and synthesis generated VHDL code using Xilinx FPGA software and generate bit file and to download bit file into FPGA hardware.

IV. FPGA TECHNOLOGY FOR MICRO-PLC

FPGA technology has great advantages to conduct the hardware controller design compared to other. The new hardware scheme of PLC can expand performance, reduce developed cost, and impose flexibility of the logic control of the manufacturing system.

The main idea is to convert the PLC program into the gate-level digital circuit expressions, only then the same control logic of the PLC represented in LD can be exactly reproduced in the FPGA-based hardware solution. Since the internal architecture of FPGA is reconfigurable, the hardware circuit can be built as long as a PLC program is converted into the Register Transfer Level (RTL) architecture and downloaded to the FPGA chip. This new solution can carry out the same functions as the original PLC and can respond to the input signals with parallel execution process at electric speed, which will improve the PLC speed. Xilinx FPGA hardware is used for PLC implementation. [1], [5]

A. Very high speed integrated circuit hardware description language (vhdl)

VHDL (VHSIC Hardware Description Language) is a hardware description language used in electronic design automation to describe digital and mixed-signal systems such as field-programmable gate arrays and integrated circuits. VHDL can also be used as a general purpose parallel programming language. VHDL is a high-level hardware description language used to describe digital circuits that can be programmed into an FPGA. [7]

V. GUI DEVELOPMENT AND LADDER DIAGRAM TO VHDL CONVERSION

A. GUI development

Figure 5 shows the Graphical User Interface which was created using Microsoft Visual Studio 2010. The user interface contains menu item toolbar, basic components as input, 10 rows X 10 columns space for ladder diagram programming. In designing the Graphical User Interface for Ladder Logic Editor, Windows Form Application (Win Form) was used. The GUI that was designed has the function of editing the Ladder Logic Diagram. The GUI has important functions, that to create, open and edit ladder logic diagram using instruction set and at last to generate VHDL code. This VHDL code is equivalent to ladder diagram.

Fig.3: Logic gate & its equivalent ladder diagram

Fig.4: Modern development environment

Fig.5: Simple Ladder Diagram (LD) create & save

Fig.6: Open VHDL code Display window
B. Ladder diagram to VHDL conversion

VI. SIMULATION RESULT

VII. CONCLUSION

For a design and develop a new micro-plc based on FPGA, implementing GUI tool base on development environment. By using the GUI tool to create, open, edit ladder diagram and then automatic convert this ladder diagram to VHDL code for a new micro-plc based on FPGA. The automatic conversion process of ladder diagram to VHDL is verify and demonstrates by simple example. This idea will be suitable for implementing a new micro-plc based on FPGA and it will give better performance and speed. It is use for smaller application where the need is limited number of function and instructions at reasonable cost.

REFERENCES


