A High Performance Design of Asynchronous Delta Sigma Modulator with High Applicability

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Abstract— Asynchronous Delta Sigma Modulator (ADSM) is playing a very crucial role in most of communicating devices and data convertor and thus requires the special attention in designing. The performance of most of the device having DSM as a primary component is characterized by the performance of the DSM circuitry. This paper presents the architecture ADSM that consumes very low power of 12.5 nW with the unity gain frequency of 48 MHz. Bandwidth of this circuit is found to be 4 MHz. A true high performance design is presented in this paper that met high performance criteria.

Key words: ADSM, Bandwidth, Hysteresis Comparator, High Performance, OTA

I. INTRODUCTION

Today is the era of low power and low voltage devices that yields high performance [1]. High performance is always modeled with respect to the technical specifications of the circuit or device. Looking at the another side of scenario, a design very accurate in high performance but very restricted to the application cannot be called truly high performance due to restriction on applications. Where a device that performs better and can be commonly used for most of the applications should be considered as high performance device with respect of customer, but the power and operating voltages as per best technical specifications should not be violated. Present techniques available for ADSM are concentrated on particular application that put restriction of usability and thus it creates need for designing multiple ADSM circuits for wide variety of application [6]. To eliminate this, one of the criteria for high performance is usability of circuit and it was be governed by the unity gain frequency and bandwidth when talking in technical sense. Today we are replacing plug n play device with the battery operated and thus low power consuming device design is necessary [5]. Keeping this in mind, low power consuming circuit is designed. For achieving low power different techniques were reviewed among which gated Vdd was found to be more suitable as it consumes very less silicon area.

Fig. 2: Architecture of High Performance ADSM
Different techniques are being researched for generating electrical energy from physical parameters such as body temperature, solar, body movements etc. voltage obtained from such sources is very low[6]. This scenario was kept in mind for designing the low voltage operating ADSM and thus it is one of the important criteria for high performance ADSM. Keeping this in mind we could say that we have given the design for future. To achieve the low operating voltages subthreshold CMOS technique was used[4]. Sub threshold devices operates at very low operating voltages typically of the order 0.25 to .5 V and thus gives new height to low operating range which was considered up to 0.8 V earlier. Some research work had been done in this regards that gives techniques for operating devices at such low voltages[5].

Fig. 1 gives the basic block diagram of Asynchronous delta sigma modulator[10]. Architecture referred here was taken from Roza’s research and will be referred as Roza’s Architecture further in this paper. As shown in the diagram, ADSM consist of an integrator followed by the hysteresis comparator, there exists a negative feed back from output to input that gives delta operation and next integrator gives sigma operation and thus referred as Asynchronous Delta Sigma Modulator. This circuit does not requires global clock for synchronization and this saves lot of circuit complexity and reduces circuit area too. Function of the ADSM is to convert analog signal to digital one but output signal is with respect to time axis only rather than with respect to discrete level. Advantage of producing output with respect to time over amplitude is that we have very fast CMOS techniques due to which we can manipulate very minute details in time rather than amplitudes[10]. When output is produced with respect to amplitude levels problem of quantization noise is observed which is not present in time domain output.

II. SUBTHRESHOLD OPERATION

Devices intended to operate at very low voltage are mostly operated in sub threshold region with bulk driven technique[6][8]. Use of this technique led to the another advantage of low power consumption as the current is very low in bulk driven weak inversion operation and low voltage low current leads to very low power consumption. IDS ie., base current of long channel MOSFET device is expressed as

\[ I_{DS} = \frac{W}{L} I_s \exp \left( \frac{q (V_{DS} - V_{TH})}{\eta kT} \right) \left[ 1 - \exp \left( -\frac{V_{DS}}{kT} \right) \right] \]

where \( I_s \) represents the characteristic current and \( \eta \) gives the slope factor in weak inversion operation. Value of \( \eta \) is given by

\[ \frac{q}{kT} + \frac{\eta_{mb}}{\eta_m} \]

and meaning of all other symbols are as per standard notations. In subthreshold region saturation occurs when \( V_{DS} > \frac{q}{\eta} \) and the threshold voltage can be given as follows

\[ V_{TH} = V_{TO} - (\eta - 1) V_{BS} \]

Relating 1 & 2, we can give

\[ I_{DS} \propto \exp \left( q \frac{V_{DS}}{kT} \right) \exp \left( q(\eta - 1) \frac{V_{BS}}{kT} \right) \]

From above we can say \( I_{DS} \) is now inversely proportional to the \( \eta \) and we can say effect of \( V_{BS} \) on \( I_{DS} \) is lowered by value \( (\eta - 1) \) as compare to \( V_{DS} \), here we point out that weak inversion operation reduces transconductance and it must be improved. The technique proposed for improving transconductance is positive source degeneration and is proposed in [6]. As shown in fig.1 a hysteresis comparator is a real comparator with finite propagation delay, this propagation delay plays very important role in deciding the centre frequency, which is reciprocal of propagation delay.
\( \tau_D \), effect of propagation delay is that, whenever voltage levels in the output of hysteresis comparator changes from or to either bound, it takes some finite time for which integrator should not integrate ideally, but this is not the case practically and integrator integrates over that period producing unnecessary transaction in output. In [3] a technique is proposed to minimize this propagation delay which is used here, details of which can be viewed from [3].

Fig. 4: Circuit Diagram for Hysteresis Comparator

III. IMPLEMENTATION

Fig. 2 shows the low power asynchronous delta sigma modulator architecture. All the transistors are identical transistors operated in weak inversion region. As shown in fig. 2 his architecture consist of a Miller Operational Transconductance amplifier proposed in [11], and a hysteresis comparator, delay element is introduced to minimize the effect of propagation delay and thus it helps to improve the centre frequency. Fig. 3 shows the implementation of advanced Miller OTA. Basic OTA designed used in this paper was proposed in [11]. Transistors used in advanced miller OTA are ensured to operate in weak inversion region with operating voltage of 0.25 V. 0.25 V operation is guaranteed by condition:

\[ V_{DS} \geq \frac{2kT}{q} \]

Source degeneration technique i.e., cross coupled transistors as shown in fig. namely Q1,Q2,Q3,Q4. Active load is contributed by \( Q_{3b} \) and \( Q_{4b} \) and \( Q_{3b} \) and \( Q_{4b} \) constitutes common gate amplifier, condition required to be ensured at \( Q_{3b} \) and \( Q_{4b} \) is biasing at

\[ V_{DS} \geq \frac{3kT}{q} \]

this ensures improvement in output impedance. Capacitor \( C_c \) serves as Miller capacitor between two stages and affects the zero frequency \( f_z \) which is given by

\[ f_z = \frac{g_{mb}}{2\pi C_c} \]

A. Hysteresis Comparator:

Hysteresis comparator used in this design is consist of bulk driven MOSFETs operated in the weak inversion region. Comparator implemented here is in the form of open loop amplifier because of which output swing is observed between \( V_{ss} \) and 0 V that is from 0.25 V to 0 V. Possibility of operating at 0.25 V can only be achieved due to use of bulk driven weak inversion operation of MOSFETs. To keep the propagation delay low hysteresis was choosen to be very small. In [6] it is guaranteed that smaller hysteresis will result in smaller HD3. Results and design for this is referred from [6].

Fig. 5: Average Power Results of High Performance ADSM
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(IJSRD/Vol. 3/Issue 02/2015/338)  

IV. RESULT

<table>
<thead>
<tr>
<th>This Work</th>
<th>[6]</th>
<th>[7]</th>
<th>[10]</th>
</tr>
</thead>
<tbody>
<tr>
<td>Technology</td>
<td>180 nm</td>
<td>130 nm</td>
<td>0.18 µm</td>
</tr>
<tr>
<td>Power Supply</td>
<td>0.25 V</td>
<td>0.25 V</td>
<td>1.8 V</td>
</tr>
<tr>
<td>Topology</td>
<td>ADSM</td>
<td>ADSM</td>
<td>DSM</td>
</tr>
<tr>
<td>Order</td>
<td>1st</td>
<td>1st</td>
<td>2nd</td>
</tr>
<tr>
<td>Input Type</td>
<td>Single Ended</td>
<td>Single Ended</td>
<td>Single Ended</td>
</tr>
<tr>
<td>Modulator Frequency</td>
<td>48 MHz</td>
<td>630 Hz</td>
<td>2 GHz</td>
</tr>
<tr>
<td>Band Width</td>
<td>4 MHz</td>
<td>30 Hz</td>
<td>1.23 MHz</td>
</tr>
<tr>
<td>SNR</td>
<td>59 dB</td>
<td>62 dB</td>
<td>79 dB</td>
</tr>
<tr>
<td>Power Consumption</td>
<td>12.5 nW</td>
<td>28 nW</td>
<td>1.8 mW</td>
</tr>
</tbody>
</table>

Table 1: Comparison of Results

Fig. 6: Frequency Spectrum of Output Signal

Fig. 7: Output Generated (Green Line) For Given Input (Yellow Line)

Circuit is simulated at 180 µm with supply voltage of 0.25 V. Fig shows the frequency spectrum of output signal and fig shows the frequency spectrum of input signal. From fig it is clear that centre frequency of 48 MHz is achieved. This frequency totally depends on propagation delay of hysteresis comparator. Fig.7 shows the measured output signal for given input signal. Peak to peak amplitude of input signal is 0.2 V. Average power consumed by circuit is 12.5 nW. Even numbered harmonics do present due to single order implementation. In order to draw conclusion we have prepared following performance comparision table as shown in table 1.

V. CONCLUSION

This work gives a circuit technique to synthesize high performance analog circuit technique that can operate on power supply of 0.25 V and consumes power <13 nW. Thus it can be concluded that high performance criteria is met successfully. Circuit achieves modulator frequency of 48 MHz with bandwidth of 4 MHz which suitable for wide range of application and thus applicability of circuit is improved.

VI. ACKNOWLEDGMENT

This research work is done by Pavan Bhagat under the guidance of Prof. Swapnili Karmore and I thank her for her guidance throughout the research.

REFERENCES

[5] Shouri Chatterjee, Yannis Tsividis, and Peter Kinget, “0.5-V Analog Circuit Techniques and


