A High Bandwidth Low Power Supply CMOS Operational Amplifier

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Abstract— In this paper, A High Bandwidth Low Power Supply CMOS Operational Amplifier (Op-Amp) is designed and analyze the effect of various aspect ratios on the characteristics, which operates at 1.2V power supply using 0.09µm CMOS technology. The Op-Amp designed is a two-stage CMOS Op-Amp. The Op-Amp is designed to exhibit a unity gain frequency of 30.87MHz and exhibits a gain of 39.86 dB. The task of CMOS Op-Amp design optimization is investigated in this work.

Key words: Operational Amplifier, 2 Stage CMOS Operational Amplifier, Stability, Scaling, Differential Amp

I. INTRODUCTION

As technology is continuously scaling to smaller transistors sizes to satisfy the market need to include more and more transistors on SRAM and DRAM and faster processing of microprocessors and microcontrollers. Due to continuous scaling sometimes analog devices performance is hampered by smaller device sizes and lower supply voltage. As the transistor length decrease, the channel modulation have a great effect and drain current increases more with a large VDS.

Op-Amps are undoubtedly one of the most useful device in the analog electronic circuitry. Op-Amp is built with vastly different level of complexity to be used to realize function ranging from a simple dc bias generations to high speed amplifications or filtering. With a handful of external components, it could perform a large number of analog signal processing tasks. Op-Amp is among the most widely used electronics device today, being used in the vast array of consumers, industries, and scientific devices. Operational Amplifiers, commonly known as Op-Amp, is one of the most widely used in Analog Electronic Circuits. Op-Amps are equally used in both analog and digital circuit.

Op-Amp is linear devices which has approximately all properties required for not only ideal DC amplification but can also be used extensively for signal conditioning, filtering and for performing mathematical operations such as addition, subtraction, integration, differentiation, multiplication, division etc. An Op-Amp is a 3-terminal device. It consists of an Inverting input denoted by a negative sign, ("-") and a Non-inverting input denoted by a positive sign ("+"). Both these inputs have very high impedance. Output of an Op-Amp is magnified difference between the two input signals. Generally the input stage of an Op-Amp is a differential amplifier.

Here our aim is to create the physical design and fabricate a low power and high bandwidth Op-amp. An ideal op-amp has a single- ended output which is characterized by a differential input, infinite voltage gain, infinite input resistance and zero output resistance. Practically these characteristics cannot be achieved. With the introduction of new CMOS design technologies of Op-Amps continue to pose challenges as the supply voltages and transistor channel lengths scaled.

The simulation is done on 90 nm CMOS technology and the Design is done in Tanner tools. After the simulation, size of most transistors still needed to be modified in order to optimize the performance. High gain of Op-Amp is not only the desired figure of merit for both analog and digital signal processing applications. Optimizing all parameters have become mandatory. The slew rate will increase with increase in current if the widths of the devices are increased with the bias voltages held constant. Thus, we can conclude that the selection of device sizes depends on trade-offs between all the parameters such as gain, bandwidth, phase margin, stability.

II. TWO STAGE CMOS OP-AMP

Op-Amp is one of the basic and most important circuits which has a wide applications in several analog circuits such as switched capacitor filters, algorithmic, pipelined and sigma delta A/D converter, sample and hold amplifier etc. The accuracy and speed of op amp circuits depends on the bandwidth and DC gain of the Op-Amp. Larger the bandwidth and larger the gain, higher the speed and accuracy of the Op-Amp circuits. These Op-Amps are one of the critical element used in analog sampled data circuit. The general block diagram of Op-Amp is shown in Fig. 1.

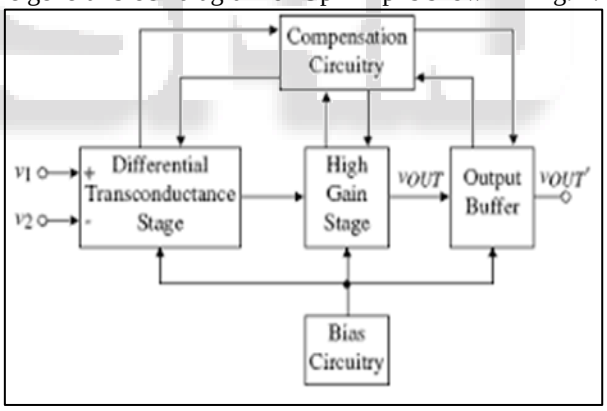

Fig. 1: Block diagram of Op-Amp

The first block in Op-Amp is a differential amplifier. It has two inputs which are named as inverting and non-inverting. The output is a differential function of the input voltages. The second block is a differential to single-ended converter. It transforms the differential signal generated by the first block into a single ended signal. Many of the applications don't require the differential to single ended function conversion so this block can be excluded. The gain provided by the input stages is not sufficient so additional amplification is required. This gain is provided by intermediate stage which is another differential amplifier and driven by the output of the first stage. As this stage use differential input and unbalanced output differential amplifier, therefore it provides extra gain. Next block is bias circuitry which is used to establish the proper operating point for each transistor in its saturation region. The next block is the output buffer stage. It provides the low output

impedance and also provides larger output current needed to drive the load of op-amp and also improve the slew rate of the op amp. Output stage can also be dropped out. If the op-amp has to drive a small and purely capacitive load, which is the case in many switched capacitor or data conversion applications then the output buffer is not used. When the output stage is not used the circuit the op amp is known as operational transconductance amplifier (OTA). The other block is compensation circuit whose purpose is to lower the gain at high frequencies and to maintain stability whenever negative feedback is applied to the Op-Amp.

A. *Circuit Operation:*

Fig. 2, shows the circuit designed to meet the required specifications. It was found that this topology was able to successfully meet all of the design specifications.

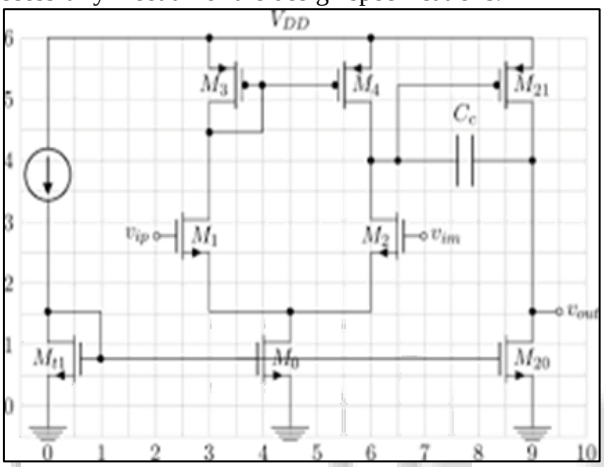

Fig. 2: The topology chosen for this Op-Amp design.

B. *Differential Gain Stage:*

Transistors M1, M2, M3, and M4 form the first stage of the operational amplifier is the differential amplifier with differential to single ended transformation. Transistors M1 and M2 are standard N channel MOSFET (NMOS) transistors which form the basic and input stage of the amplifier and the W/L ratio of all these MOSFET are also varied. The gate of M1 is the inverting input and the gate of M2 is the non-inverting input. A differential input signal applied across the two input terminals will be amplified according to the gain of the differential stage. The gain of the stage is simply the transconductance of M2 times the total output resistance seen at the drain of M2. The two main resistances that contribute to the output resistance are that of the input transistors themselves and also the output resistance of the active load transistors, M3 and M4. The current mirror active load used in this circuit has three main advantages. Firstly, the use of active load devices create a large output resistance in a relatively small amount of die area. Secondly, the current mirror topology performs the differential to single-ended conversion of the input signal and lastly, the load also helps with common mode rejection ratio. In this stage, the conversion from differential to single ended is achieved by using a current mirror (M3 and M4). The current from M1 is mirrored by M3 and M4 and subtracted from the current from M2. The differential current from M1 and M2 multiplied by the output resistance of the first stage gives the single-ended output voltage, which constitutes the input of the second gain stage.

C. *Second Gain Stage:*

The second stage is a current sink load inverter. The purpose of the second stage is to provide additional gain in the amplifier. Consisting of transistors M20 and M21, this stage takes the output from the drain of M2 and amplifies it through M21 which is in the standard common source configuration. Again, similar to the differential gain stage, this stage employs an active device, M20, to serve as the load resistance for M21. The gain of this stage is the transconductance of M21 times the effective load resistance comprised of the output resistances of M21 and M20. M20 is the driver while M0 acts as the load.

III. PROPOSED WORK

The proposed design is a two-stage op amp with an n-channel input pair. The Op-Amp uses a dual-polarity power supply (Vdd and Vss) so the ac signals can swing above and below ground and also be centered at ground. Schematic used in this design is shown in Fig. 3.

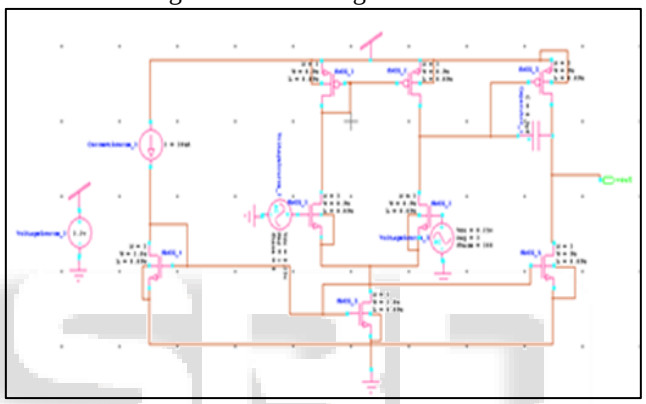

Fig. 3: Schematic of Operational Amplifier

IV. SIMULATION RESULTS

Simulation results are shown in Table I. Gain of the Op-Amp is 39.86 dB after calculation and also shown in Fig. 4. Bandwidth of the proposed Op-Amp is 30.87 MHz which is shown in Fig. 5.

Name of parameter	Value of parameter
Technology	90 nm
Power Supply	1.2 V
Capacitor	0.01 pF
Gain	39.86 dB
Offset Voltage	300mV
Bandwidth	30.87 MHz

Table 1: Simulation Result

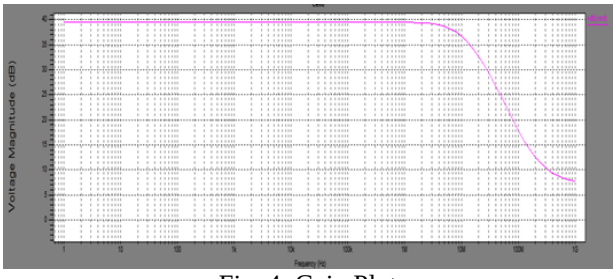

Fig. 4: Gain Plot

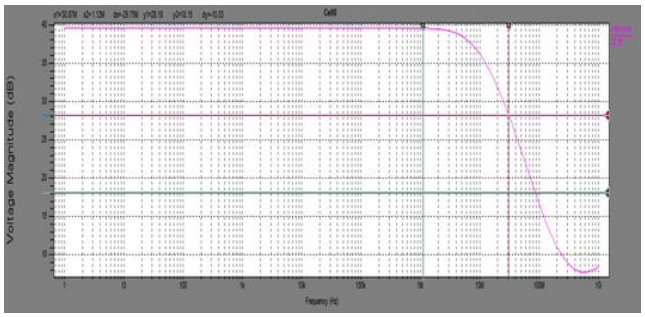

Fig. 5: Calculation of bandwidth using Gain plot

V. CONCLUSION

The designed Op-Amp has the high gain and bandwidth which are the requirement of a high performance Op-Amp. Here, we used only 1.2V power supply which makes designed Op-Amp low powered. So, power dissipation is also low for this design. We have 39.86 dB gain which makes this design suitable for high frequency applications.

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