Power Gating Based Low Power 32 Bit BCD Adder using DVT

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Abstract— Minimizing power dissipation during the VLSI design flow increases life time and reliability of the circuit. Numerous technologies for the design of low power VLSI circuits are reported where the dominant factor of power dissipation is caused by switching activity and large circuit area. The techniques used to reduce the power consumption and leakage power in a circuit is DVT and Power Gating. The GDI technique consumes low power which is used to design a full adder in a circuit. The simulation is done by using TANNER (EDA) tool and the result is compared with other BCD adder circuits. The average power consumed by the BCD adder is 1.384 µw and the frequency is 200 MHZ with 1v supply voltage.

Key words: Binary coded decimal (BCD), ElectronicDesign Automation (EDA), Gate Diffusion Input (GDI), DVT (Dual Voltage)

I. INTRODUCTION

A. *BCD Adder:*

The BCD system was chosen for the internal number system in many computers because it is easy to convert it to alphanumeric representations for printouts and displays. The main building block of BCD adder is full adder. It is used to produce binary addition result. If the obtained result is below 9 then no need of correction required. If the obtained result excess of 9 then the decimal number 6 is added with the result for correction. The full adder is basically a ripple carry adder. The output of one full adder circuit is applied into input of other full adder circuit.

B. *Power Gating:*

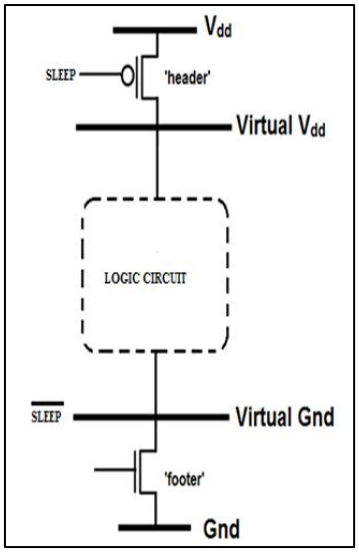

Fig. 1: Power gating

Power gating is a technique used in digital circuit design to reduce power consumption, by turning off the current to entering the blocks of the circuit while that are not in use. Power gating uses low-leakage PMOS transistors as header switches to shut off power supplies to parts of a design in standby or sleep mode. NMOS footer switches can also be used as sleep transistors shown in Fig 1. Inserting the sleep transistors splits the circuit's power network into a permanent power network connected to the power supply and a virtual power network that drives the cells and can be turned off.

C. *GDI Technique:*

This technique allows reducing various parameters like power consumption, propagation delay, and area of circuits. A basic GDI cell shown in Fig 2 contains four terminals namely– G (common gate input of Nmos and pMOS transistors), P (the outer diffusion node ofpMOS transistor), N (the outer diffusion node of nMOS transistor), and D (common diffusion node of both transistors).Basically the design looks like an inverter, but the main differences are (i) GDI consist of three inputs- G (gate input to NMOS/PMOS), P (input to source of PMOS) and N (input to source of NMOS). (ii) Bulks of both NMOS and PMOS are connected to N or P (respectively), so it can be arbitrarily biased at contrast with CMOS inverter. This design can implement a wide variety of logic functions using only two transistors. This method is suitable for design of fast, low-power circuits, using a reduced number of transistors.

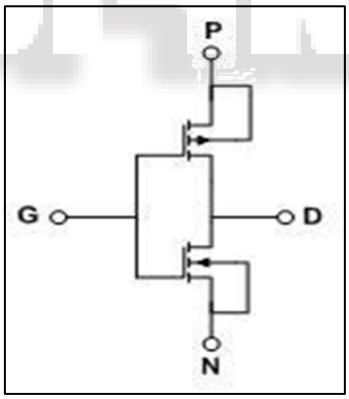

Fig. 2: Basic GDI cell

II. GDI TECHNIQUE IN BCD ADDER

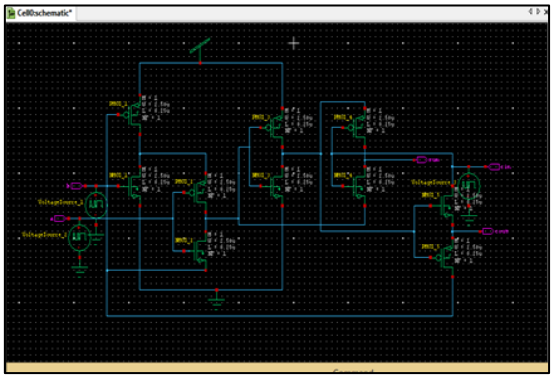

Fig. 3: 1-Bit full adder using GDI

Full adder is the main building block of BCD adder. So the power full adder is designed using GDI technique. It contains only 10 transistors for 1-bit full adder. By using this 1-bit full adder 32-bit full adder is designed shown in Fig 3 and the corresponding block diagram is shown in Fig 4.

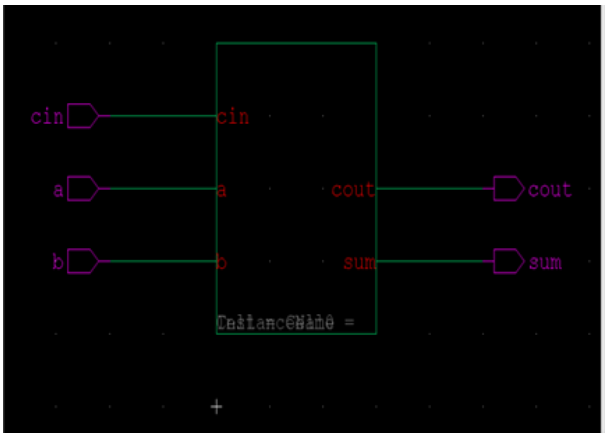

Fig. 4: Block diagram of 1-Bit full adder

The input of the full adder is a, b, cin respectively and the outputs are sum and carry. To obtain a 32-bit full adder shown in Fig 6, the 1-bit full adders connected in ripple carry adder format. That is the carry output of one full adder is given as input of the other full adder shown in Fig 5.The layout of a ripple-carry adder is simple, which allows for fast design time.

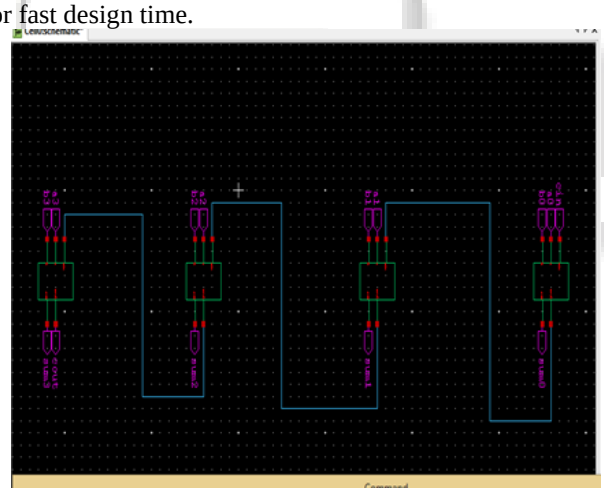

Fig. 5: Block diagram of 4-Bit full adder

A	B	C_{in}	C_{out}	S
0	0	0	0	0
1	0	0	0	1
0	1	0	0	1
1	1	0	1	0
0	0	1	0	1
1	0	1	1	0
0	1	1	1	0
1	1	1	1	1

Table 1: Truth Table of 1-Bit Full Adder

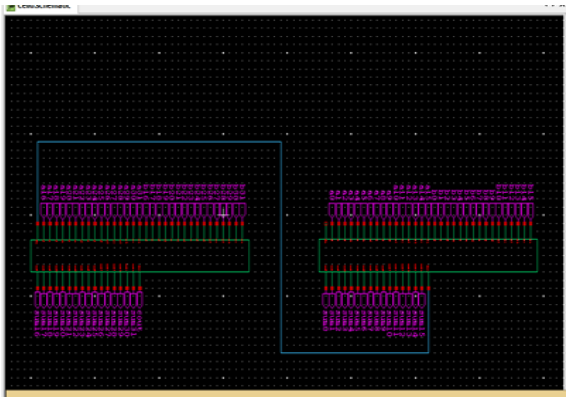

Fig. 6: Block diagram of 32-bit full adder

III. POWER GATING IN BCD ADDER

The power gating technique is also applied to the full adder. The Pmos is connected at the top of the circuit and the Nmos is connected at the bottom of the circuit. The inputs of that Pmos and Nmos are SELECT, SELECT' respectively. By activating the SELECT input the header part of the circuit's power consumption is controlled when the circuit is in idle. Similarly for footer circuit also but vice versa.

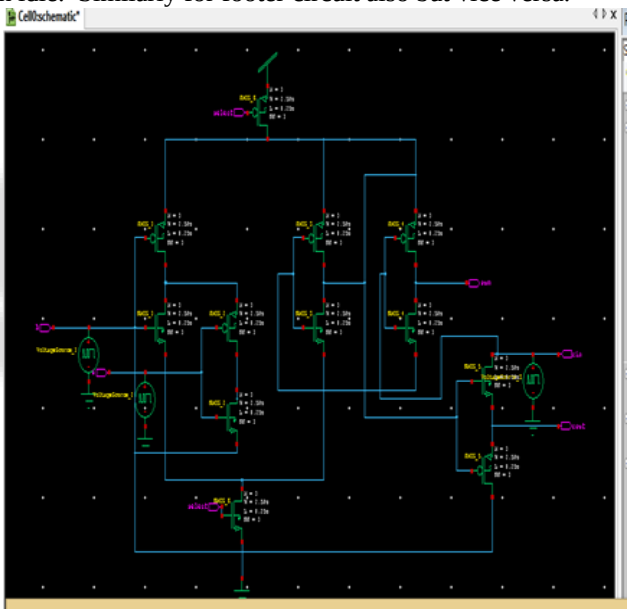

Fig. 7: 1-Bit full adder circuit with power gating

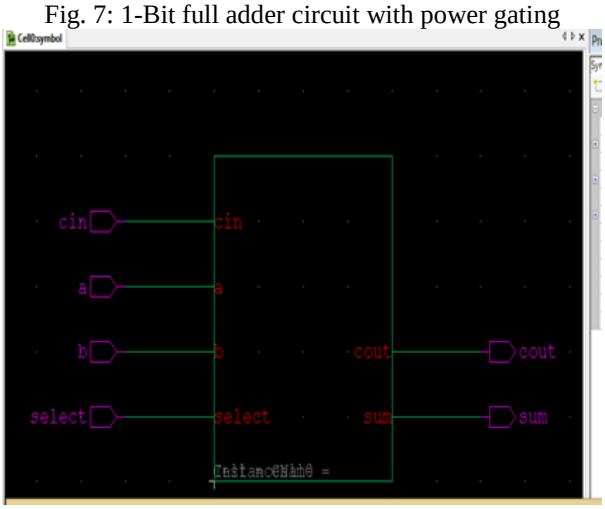

Fig. 8: Block diagram of 1-bit full adder with Power gating

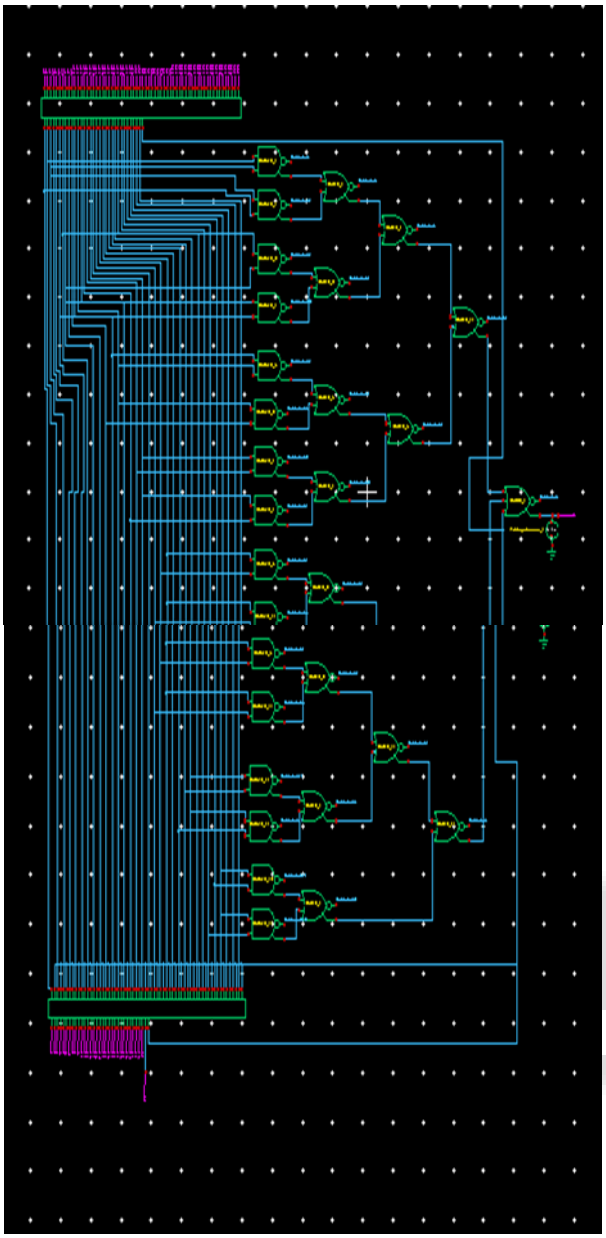

Fig. 9: 32-Bit BCD adder with Power gating

IV. SIMULATION RESULTS

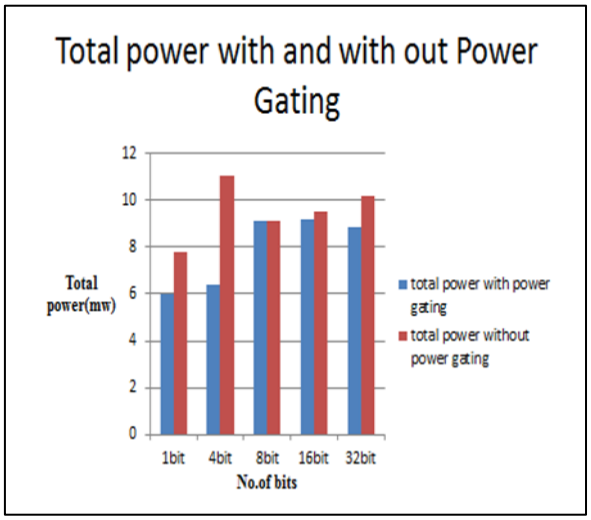

Fig. 10: Comparison Graph of With and Without Power Gating

The simulation result of with and without power gating of 1-bit to 32-bit full adder is obtained by using T-spice in TANNER EDA tool. The power is calculated using T-spice command window by using the command .power VVoltageSource_[name].

Parameters	Existing Method	Proposed Method
No of Bits	4	32
Transistor Count	16(for 1-bit)	10(for 1-bit)
Technology	40nm	IBM013
Method for full adder design	Conventional full adder	GDI technique
Power	60%	80%
Delay	55%	70%
Supply voltage	5V	1V
Operating Frequency	200Hz	200Hz
Performance	Low	High
Speed	Low	High

Table 2: Comparison Table of Existing and Proposed Method

No. of bits	Sum (mw)	Carry (mw)	Total (mw)
1-bit	2.141	5.67	7.81
4-bit	5.54	5.517	11.05
8-bit	3.82	5.30	9.12
16-bit	4.20	5.299	9.499
32-bit	4.88	5.297	10.177

Table 3: Power Calculation of full adder without Power gating

No.of bits	Sum (mw)	Carry (mw)	Total (mw)
1-bit	2.121	3.901	6.02
4-bit	2.429	3.953	6.37
8-bit	4.86	4.3022	9.1
16-bit	4.84	4.323	9.16
32-bit	4.80	4.027	8.827

Table 4: Power Calculation of full adder with Power gating

V. CONCLUSION

Power is the important factor in modern electronic world. The power and area are directly proportional to each other. If the area of the circuit is large the power consumption is also large. So the full adder used in BCD adder is designed with GDI technique and the full adder used RIPPLE CARRY adder because of its small circuit area and delay. The simulation result is done using TANNER EDA with 130 nm technology. The design of full adder is important consideration in BCD adder. So the full adder in BCD adder is designed by using GDI technique. By using simulation result the parameters like average power, delay and power delay product are measured and it is compared with other techniques.

A. The Future Work Includes:

The DVT (Dual Threshold Voltage) method is also applied in the design to minimize leakage power. So the power consumed by the circuit is furthermore reduced compared to that of existing methodology circuit.

VI. REFERENCES

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