Low Power High Performance Conditional Pulse Triggered Flip Flop

Anuka[1] Shalley Garg[2]
[1]M.Tech Student [2]Professor
[1,2]Department of Electronics & Communication Engineering
[1,2]Indus Institute of Engineering and Technology, Kinana, Jind, Haryana – 126102

Abstract— In this work, a Low Power High Performance Conditional Pulse Triggered Flip Flop is proposed. The proposed design fulfills the discharging problem using the pulse generation circuit with modified delay circuit. A three-transistor inverter design is used to reduce the circuit complexity, delay and speed up the discharge along the critical path when circuit needs. Modified scheme is used different approach to provide delay in the clock (CLK). As a result, no. of transistor reduces in pulse-generation circuit and delay inverter provides lower power dissipation. All simulation results are based on using CMOS 90-nm process technology at 500MHz clock frequency. Tanner 14.1 software is used for simulation process. Its maximum power saving against signal feed through FF is up to 37.3%

Key words: Flip-flop, Low Power, Conditional Pulse Triggered

I. INTRODUCTION

Flip flops (FFs) are used as the main storage elements in most of the digital devices such as register files, counters and shift registers. It is estimated that the power consumption of the clock system, which consists of clock distribution networks and storage elements, is as high as 49-50% of the total system power [1]. FFs contribute a large portion of the chip area and power consumption to the overall system design. Due to the single latch structure of pulse-triggered FF (P-FF), it is more popular than the conventional transmission gate (TG) and master–slave predicated FFs in high-speed applications. Besides the speed advantage, its circuit simplicity lowers the power consumption of the clock tree system. A P-FF consists of a pulse used for strobe signals and a latch used for data storage. If the triggering pulses are very narrow, then latch acts like an edge-triggered FF [2]. Since only one latch is needed for a P-FF than two used in the conventional master–slave configuration. This leads to a higher toggle rate for high-speed operations. P-FFs withal sanction time borrowing across clock cycle boundaries and feature a zero or even negative setup time. Regardless of these advantages, pulse generation circuit requires delicate pulse width control to deal effective with possible variations in process technology and signal distribution network [3]. In this, a statistical design framework is developed to take these factors into account. To obtain better performance among delay, power and area, design space exploration is withal a widely used technique.

In this paper, we have presented a low-power high performance conditional pulse triggered FF design with modified clock pulse generation circuit. In the second section, we present the previous pulse-triggered flip-flops. In the third section, we present the proposed flip-flop with description. In the fourth section, we show the simulation results with comparison table. And in last section, we conclude the results.

II. CONVENTIONAL FLIP-FLOP

The conventional flip-flops [1] are shown in the Fig.1. In all the conventional FFs, same CLK Pulse Generator (PG) circuit is used except Modified Hybrid Latch Flip Flop (MHLFF). CLK PG contains NAND gate, three delay inverter and one inverter at the output of NAND gate to make it AND gate. . When CLK=0 and CLKbar=1, then NAND gate output is "1" and Pulse_CK=0. And when CLK=1 and CLKbar=0, then NAND gate is also "1" and Pulse_CK=0. But when CLK goes to "0" to "1" means rising edge of the CLK occurs, then CLKbar remains "1" due to the delay provided by three inverters in series. It will generate CLK pulse to control the FF. All these FFs have the basic phenomena of Data (D) FF means input is transferred to the output with the help of CLK. From these 5 FFs, signal feed through technique [1] is the best technique for the FFs. Transistor MNx is the main controlling transistor during charging and discharging of the output node Q. When Q_fdbk=1 and Data is also "1", then at the rising edge of the CLK, node X discharges through MN1, MN2 and MN3 transistors. And makes transistor MP2 ON that starts charging node Q, but at the same time, MNx is ON due to Pulse_CK is applied at their gate terminal. It will push the node Q to charge quickly. When Data=0 and rising edge occurs, then node Q discharges through MNx transistor to input Data. But it has high power dissipation due to transistor MP1 is always ON during discharging of node X. In the proposed design, we will remove this problem.

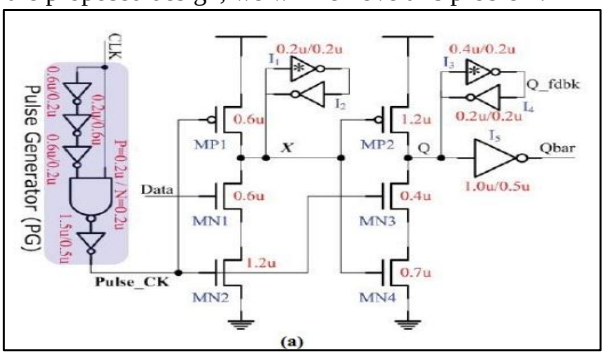

Fig. (a):

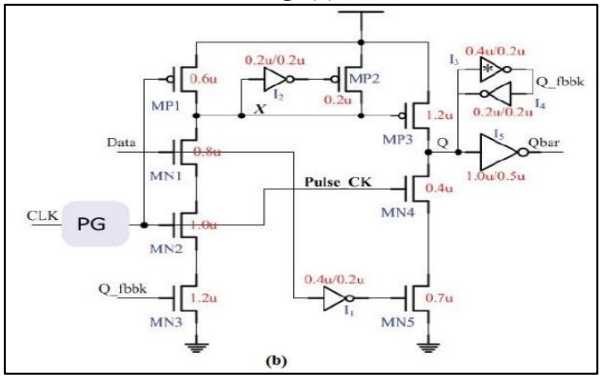

Fig. (b)

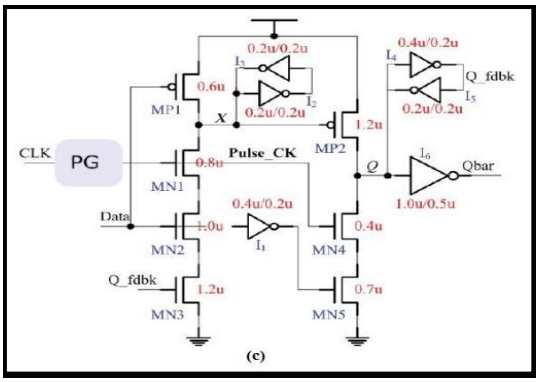

Fig. (c):

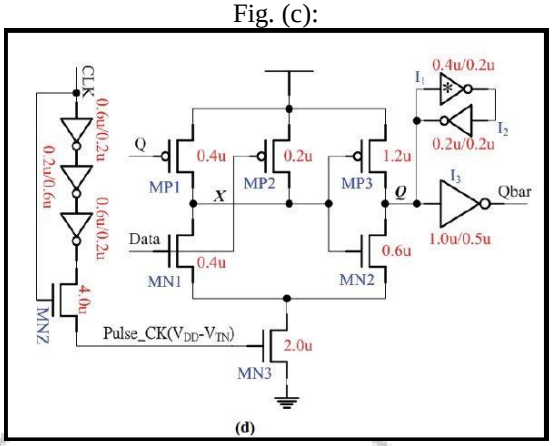

Fig. (d):

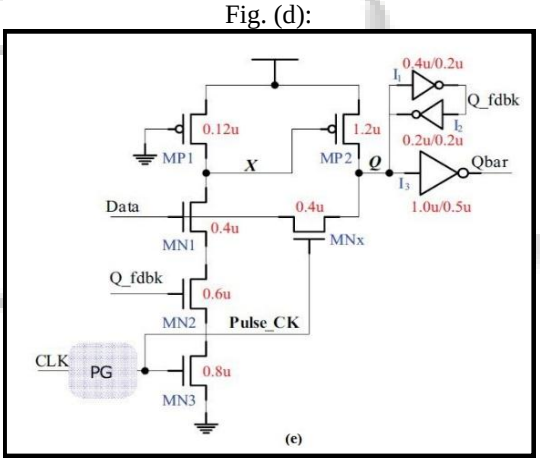

Fig. (E):

Fig. 1: Conventional FFS Design A) Ep-DCO B) CDFF C) Static CDFF D) MHLFF E) Signal Feed Through FF

III. PROPOSED WORK

Proposed FF is shown in Fig. 2(a). New FF design, with the new clock pulse generator which has the modified inverter (Fig. 2(b)), is described below. In this clock pulse generator, Inverter I1 is designed in such a way that delay is created in CLK due to extra transistor N6 at the rising edge of the CLK. It provides better CLK Pulse (CP) (in height and width) than the previous FF CP. So it reduces the power consumption and delay in the proposed flip-flop. When CLK=0 and CLKbar=1, then NAND gate output is "1" and CP=0. And when CLK=1 and CLKbar=0, then NAND gate is also "1" and CP=0. But when CLK goes to "0" to "1" means rising edge of the CLK occurs, then CLKbar remains "1" due to the delay provided by inverter I1. So, NAND gate output goes low and we get CP=1 for some time. It generates CP at the rising edge of the CLK. This CP controls the discharging of node X & Q and charging of node X. Let initially Q=0, so Qbar=1 means transistor N1 is ON. When CP=0, transistor P1 is ON and it charges node X. If Data=1 and CLK rising edge occur, then transistor N2 and N4 are ON, and node X is discharged through N1, N2 and N4 transistors. It switches ON P2 transistor that will charge the output node Q. It means when Data=1, then Q becomes "1" at the rising edge of the CLK. When Data=0, then Db=1 that makes transistor N3 ON. At the rising edge of the CLK, node Q will discharge through transistor N3 and N4. In the previous design, transistor P1 is always ON due to ground applied at the gate terminal. So, it dissipates more power during the switching of the node X. But in new design, transistor P1 is almost OFF during the discharging of the node X that lowers the power dissipation in the proposed FF.

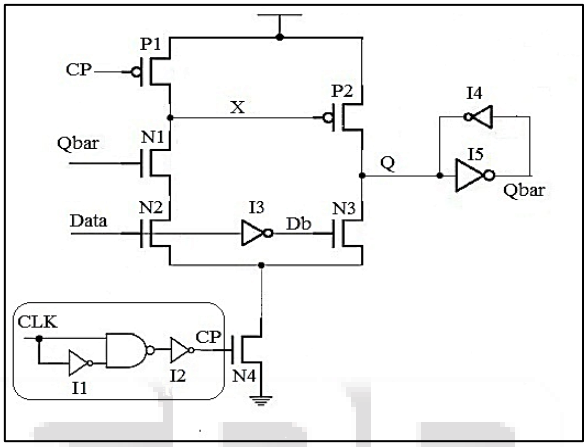

Fig. (a) Proposed FF

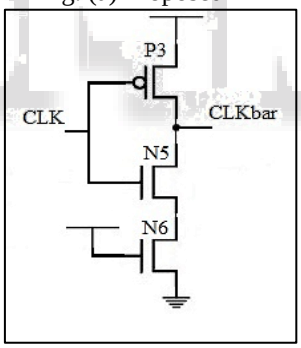

Fig. (b) Modified Inverter I1 design

Fig. 2: (a) Proposed FF (b) Modified Inverter I1 design

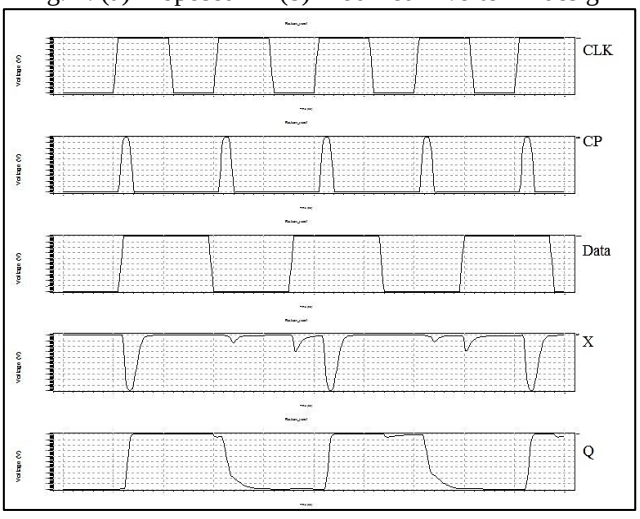

Fig. 3: Proposed FF Simulation Waveform

Flip-Flop	epDCO	CDFF	Static CDFF	MHLFF	Signal feed through FF	Proposed FF
No. of Transistors	28	30	31	19	24	21
D-to-Q Delay (ps)	147.65	148.11	153.30	171.27	140.51	137.13
Power (100% Switching) uW	26.537	28.970	27.266	25.108	23.312	18.117
Power (50% Switching) uW	25.762	24.587	23.654	20.342	19.854	13.449
Power (25% Switching) uW	21.692	20.447	21.101	18.298	16.775	10.503
PDP (50% Switching) fJ	3.80	3.64	3.62	3.48	2.78	1.84

Table 1: Performance Comparison Table of Different FFS

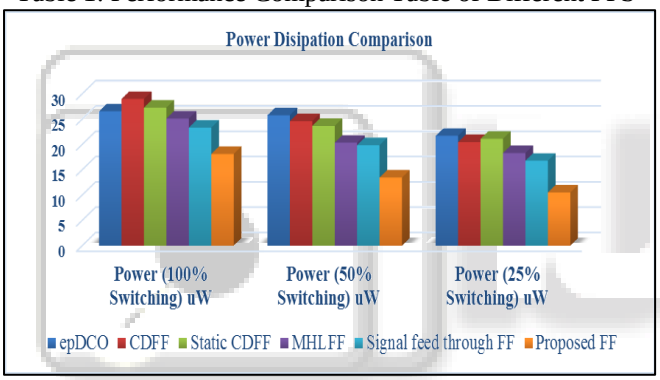

Fig. 4: Power Dissipation Comparison of FFS at Different Switching Activities

IV. Simulation Results

Conventional FF is described in section II and proposed FF is explained in section III. All simulations have carried out at 90nm process technology, 1V power supply and 500MHz clock frequency with the 100 %, 50% and 25% switching activity of the Data with respect to CLK. A 15fF capacitor has been loaded at the output of the FFs. Comparison of the both FFs are shown in Table I which contains the power dissipation at different switching activity, Data-to-Q delay, no. of transistors and power-delay product (PDP). Simulation waveforms are shown in Fig. 3. Power dissipation comparison of conventional and proposed FF at different switching activities is shown in Fig. 4.

V. Conclusion

In this paper, we designed a low-power high performance conditional pulse-triggered FF design with modified conditional pulse enhancement scheme by employing one new design measures. This successfully reduces the number of transistors in the CLK pulse generator circuit with modified inverter to make proper height and width of the pulse so that the size of the transistors in the pulse generation circuit can be kept minimum. One inverter is removed at the output of the FF which is used for Qbar. Here, we used the bistable circuit (two inverters are connected back to back) for the Qbar and to maintain Q stable [6], [8]. Proposed design has maximum power saving against signal feed through FF up to 37.3%.

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