Design and Analysis of Leakage Power Reduction Circuits for Various Power Gating Architectures

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Abstract— The design of low power circuit has begun to be a prime concern in chip design, substantially for portable and high performance systems. Power reduction is one of the mandatory issues. Scaling the transistor size causes sub-threshold leakage currents to become a massive component of total power dissipation. Therefore, effective techniques are required to minimize leakage power. Here we are going to design the multi-mode power switches based on various modes in power gating architectures. Multi-Threshold CMOS (MTCMOS) has appeared as an effective power gating technique in which standby sub-threshold leakage is minimized by interrupting power of the idle blocks by placing of sleep transistors. We propose a dual stack and body-biasing techniques with power gated circuits. The implementation of reconfigurable architecture provides reduced power and delay. TANNER EDA tool is used to design and verify the architectures.

Key words: Leakage Power, Power Gating Circuits, Multi-Threshold CMOS, Dual Stack, Body-Biasing

I. INTRODUCTION

The primary goal of VLSI technology is to minimize the power dissipation. In [7], the usage of battery-powered hand-held applications like mobile phones, note pad and laptop computers is steadily increased and more number of applications are integrated into single device which is also a reason to reduce the power consumption. Static and dynamic power dissipation is the two main types which causes power dissipation. When the device is in power down mode static power dissipation becomes an issue. Dynamic power dissipation occurs when the circuit is working, i.e. the circuit is performing some task on some data.

On the report of ITRS, static power becomes more important with device scaling. The total power consumption in chip is mainly due to the leakage power as technology feature size shrinks [1]. Hence reducing leakage power is important than reducing static and dynamic power in the total power consumption without trading off system performance. Several techniques are suggested for reducing leakage current. The main contribution of leakage power dissipation involves reversed biased diode leakage and sub-threshold leakage currents [9]. If the threshold voltages scale down, sub threshold leakage will be conspicuous. The transistors will not be entirely off under the threshold voltage, in weak inversion. The threshold current is strongly influenced by the sub threshold voltage.

As stated in modern CMOS, if circuits are idle, leakage mechanisms start to evacuate current. Even at smaller geometry processes, leakage power consumption is larger than dynamic power consumption. Hence we should introduce new design techniques to prevent leakage power.

II. BACKGROUND

Minimizing power consumption is the major thrust towards designing of integrated circuits while trading off system performance. There are many techniques for reducing leakage power in sleep or active mode. Power gating technique is one such conventional technique that uses the power supply voltage as the primary source. The power gating switch is typically arranged as header between the circuit and the power supply rail or as footer between the circuit and the ground rail [3]. During active operation, the power gating switch remains on, supplying the current that the circuit uses to operate. During standby mode, the device will turn off the power gating switch to reduce the leakage path through the circuit. Turning off the sleep transistor provides substantial leakage reduction with less impact on performance.

In power gating circuit, during the time of sleep transistor off condition, the ground rail charges up to the value close to supply voltage. However, it has the demerit that while switching back to normal (active) mode from sleep mode, the ground rail takes much time. Hence it limits the savings of over all leakage and results in wake-up latency and penalty [10]. Thus, it is sensible to have multiple sleep modes for short period of inactivity.

III. POWER GATING ARCHITECTURE

Power gating architectures with three different modes of operations [10] have been illustrated in Fig.1. It mainly contains three transistors Mps (power switch transistor), M0 and M1 (intermediate power-off modes). M1 indicates the dream mode and M2 indicates the sleep mode. In the core area insertion of NMOS is preferable, because NMOS on-resistance is less comparing to PMOS.

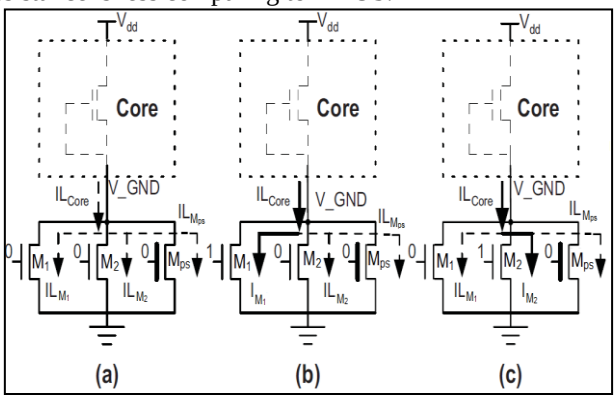

Fig. 1: Power Gating Architectures (A) Snore Mode (B) Dream Mode (C) Sleep Mode

M_{ps} is a high-V_t and it will be ON when it is in active mode. Low- V_t transistors are M_1 and M_2, It will turn ON during dream mode and sleep mode respectively. This architecture is tolerance to task (process) variations. It

absorbs less static power, as it is furnished with two or more intermediate power off modes. Thus the working of this type is more definable. In the end, a power gating circuit with reconfigurable version is also introduced.

IV. RECONFIGURABLE ARCHITECTURE

The reconfigurable architecture [2] is shown in Fig.2. In this structure, we combine two different modes from power gating architecture, namely sleep mode and dream mode. For even more process variations, each transistor M_1 and M_2 are exchanged with triplet of transistors (M_1^-,M_1, M_1^+), (M_2^-,M_2, M_2^+) respectively.

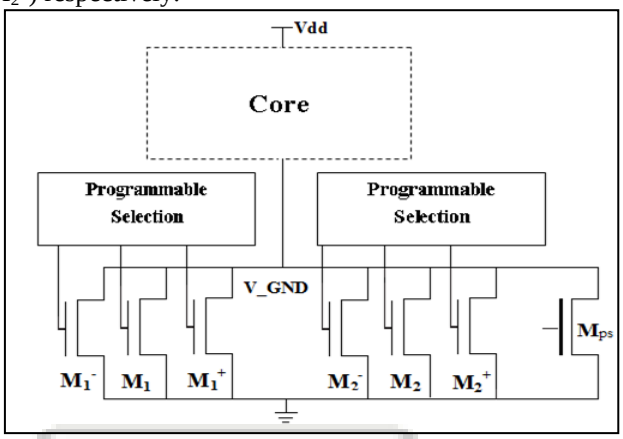

Fig. 2: Reconfigurable Architecture

In [2] Programmable structure is use to select each triplet transistors, which allows the utilization of the power gating architecture for newer technologies. One of the advantage of this circuit is, it can be easily modified. During standby mode, it is used to reduce sub-threshold currents by maintaining circuit performance.

A. MTCMOS Technique:

The effective and commonly used power gating mechanism to reduce leakage power is Multi-Threshold CMOS (MTCMOS) [4]. It uses multiple threshold voltages to optimize power. It contains high-V_{th} device and a low-V_{th} computational block which is power gating circuit. One type of high-V_{th} switch is enough for power gating [3].

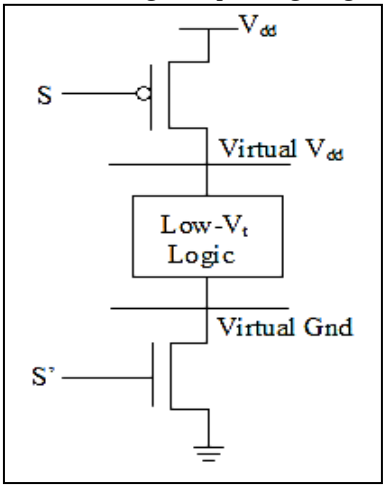

Fig. 3: Multi-threshold Voltage CMOS (MTCMOS)

As illustrated in Fig. 3, two sleep transistors S and S' are added, PMOS transistor as header switch and NMOS transistor as footer switch. In fact, for leakage reduction only one type of high Vth transistor is suitable.

Even though, MTCMOS can reduce leakage power, it can increases area and delay significantly. Moreover, an additional high Vth memory circuit is needed to maintain the data, when data retention is required in standby mode. It is not suitable for sequential circuits [5].

V. PROPOSED WORK

The reduction of leakage power is the major issue in VLSI technology. There are some techniques in VLSI to minimize leakage power. Each mechanism yields a logical way to lessen leakage power but demerits of every technique restrict the implementation of each one. We propose new approaches, namely dual stack and body biasing which provides a new option to decrease leakage power for VLSI designers.

A. Dual Stack Technique:

A new approach to decrease leakage power is the dual stack [8]. This technique is based on a stacking, by splitting an existing transistor into two halves. This stack approach [9] merges the sleep and stacking approaches. After the division of two halves, sleep transistors are connected in parallel with divided transistors.

In saving state of sleep mode, transistors S and S' are turned off and stacked transistors extinguish leakage current. For every sleep transistor, stacked transistors connected in parallel with it. Which minimizes resistance path, hence delay is decreased throughout active mode. But, area penalty in NMOS is a consequence to this approach.

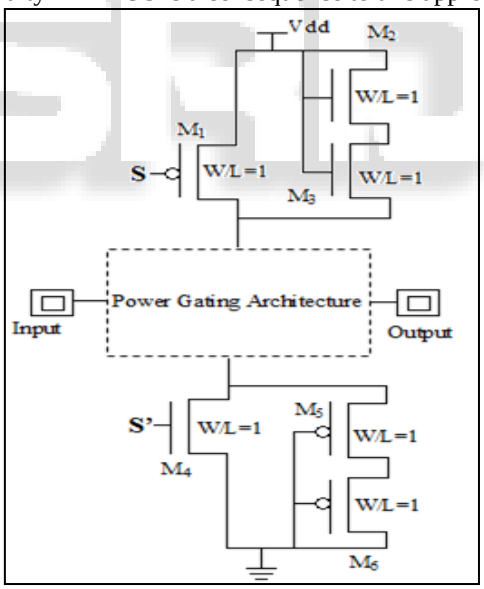

Fig. 4: Dual Stack Technique

As shown in fig. 4, The dual stack approach uses two additional PMOS in the footer switch and two additional NMOS in the header switch, S and S' are sleep transistors. The power gating architecture is stacked between S and S' transistors. As a result, NMOS and PMOS decay the corresponding high and low logic level. Because of the body effect they decrease the voltage level for greater extent. So, the pass transistor reduces the voltage applied across the main circuit. The transistors are stacked and carried in reverse body bias. Hence the result will be high threshold. Low leakage current can be done by high threshold voltage and thus low leakage power is established.

B. Body Biasing Technique:

To provide greater efficiency, a body biasing technique [6] is implemented, by rescuing performance lost by variations. The power gating modes are connected between S and S' sleep transistors. In the sleep mode we have to degrade the leakage current. To get a minimized leakage current, body to source voltage of the sleep transistor should be maximized.

When V_{bs} increases, current leakage will be reduced to a great level. Due to the body bias effect PMOS (M_2) source is connected to the body of the PMOS (M_1) and a NMOS (M_5) is connected to the NMOS (M_4), this is shown in Fig.5. In the case of sleep mode PMOS ($M_{2)}$ will be in OFF condition so the body to source voltage of the PMOS (M_1) is greater than in the active mode. This similar discussion is used for the NMOS (M_4 and M_5). In sleep mode the PMOS (M_6) and NMOS (M_3) works together to retain the state.

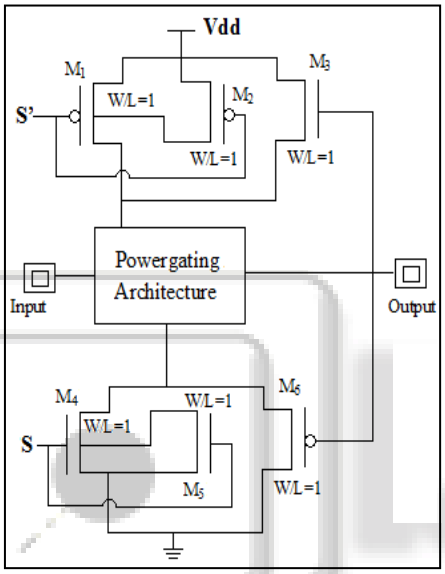

Fig. 5: Body Biasing Technique

This technique additionally uses PMOS (M6) and NMOS (M3) in the pull down and pulls up network respectively and both networks are parallelized to the corresponding sleep transistors while maintaining the state in sleep mode.

As a result of Body effect, V_{th} also increases which lowers the performance. During the active mode, the performance is improved as the PMOS (M_2) is ON which makes the V_{th} of the pull up PMOS (M_1) lower again. The original propose of the substrate biasing was utilized to reduce sub-threshold leakage during standby mode in portable applications. More recently, it has been employed to reduce the maximum power dissipation by lowering V_{th} (forward body biasing) in active mode, and by compensating V_{th} variations.

VI. SIMULATION RESULTS

The schematic of conventional and proposed power gating with reconfigurable architectures are designed and implemented by using TANNER EDA tool. The circuits are characterized by using the 90nm technology. The parameters power and delay compared between each techniques.

Fig. 6 to Fig.13 shows the schematic diagram and output waveform for each leakage power reduction techniques. Fig.14 shows the comparison chart of static power consumption. Fig. 15 shows the comparison chart of propagation delay.

Table.I lists static power consumptions by the synthesis report of power gating architectures with leakage power reduction techniques. Table.II lists the comparisons of propagation delay with each technique.

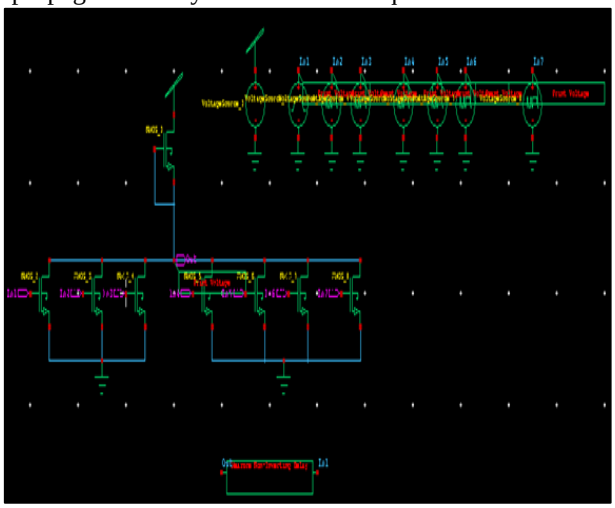

Fig. 6: Design of Reconfigurable Architecture

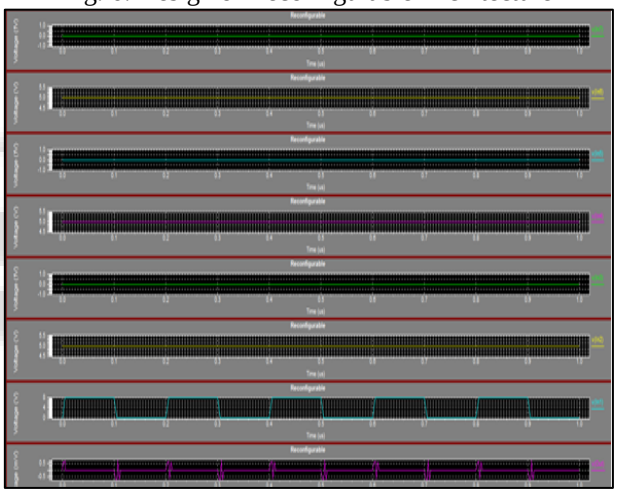

Fig. 7: Output Wave Form for Reconfigurable Architecture

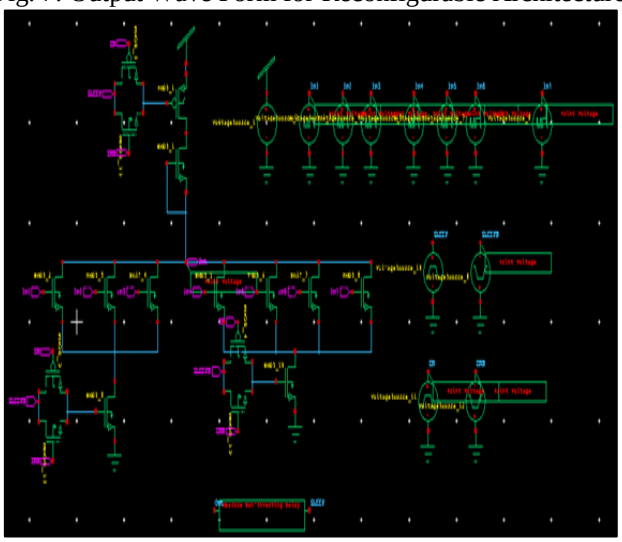

Fig. 8: Design of Reconfigurable_MTCMOS

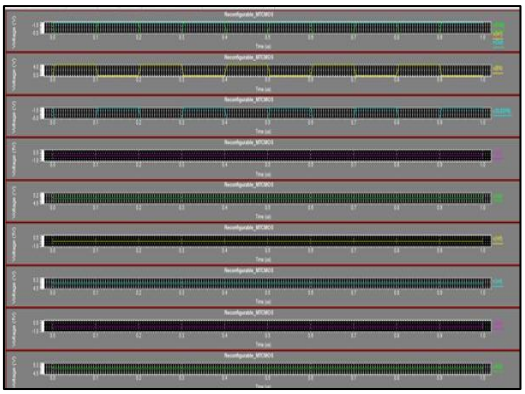

Fig. 9: Output Wave Form for Reconfigurable_ MTCMOS

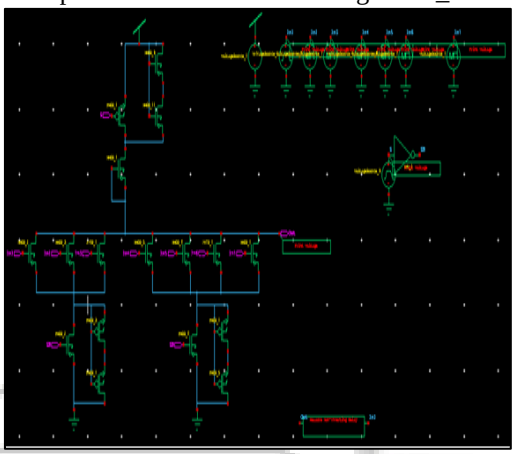

Fig. 10: Design of Reconfigurable_Dual Stack

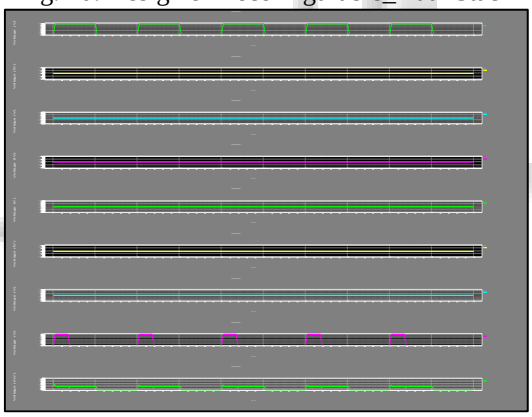

Fig. 11: Output Wave Form For Reconfigurable_ Dual Stack

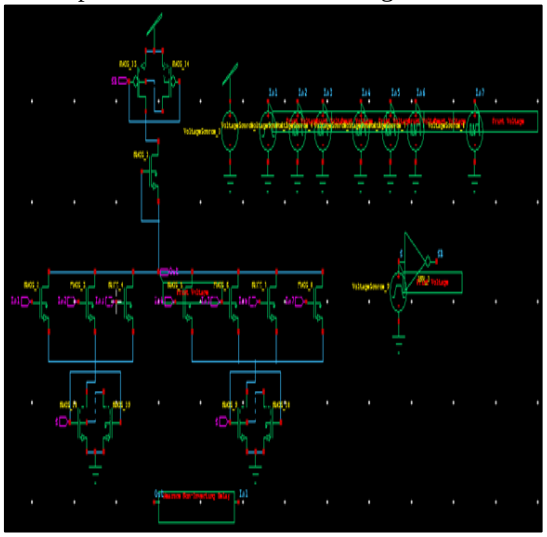

Fig. 12: Design of Reconfigurable_Body-Biasing

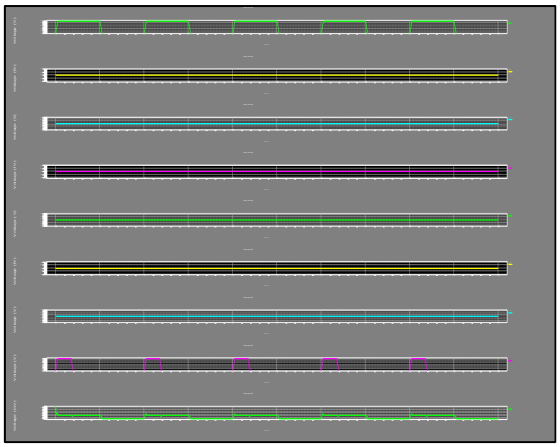

Fig. 13: Output Wave Form for Reconfigurable_ Body Bias

POWER GATING MODES	POWER(µw)			
	SWITCH MODES	MTCMOS	DUAL STACK	BODY BIAS
DREAM	4.8788	3.0426	2.1165	1.9508
SLEEP	5.9742	4.0104	3.2095	2.6336
SNORE	6.2295	6.1334	4.2209	1.9968

Table 1: Power Consumptions of Power Gating With Different Techniques

CIRCUIT NAME	POWER (µw)	DELAY (ps)
Reconfigurable	3.9522	5.2500
Reconfigurable_MTCMOS	3.2654	2.7500
Reconfigurable_DS	2.6726	2.5000
Reconfigurable_BB	1.9941	2.0000

Table 2: Power And Propagation Delay of Reconfigurable Architectures

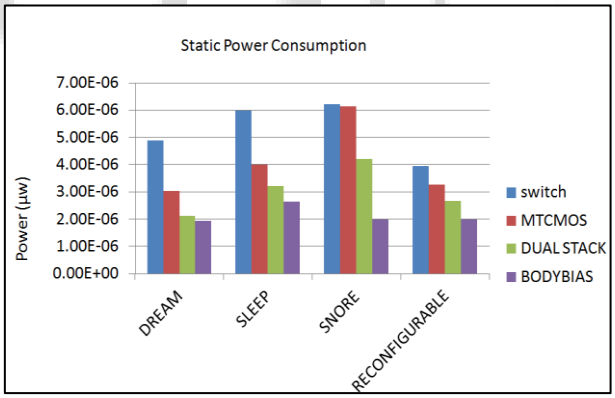

Fig. 14: Static Power Comparison

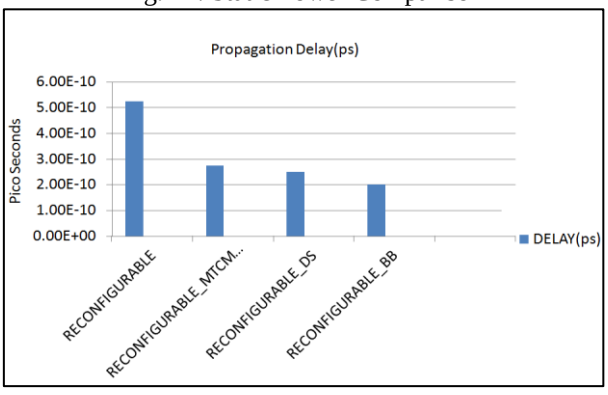

Fig. 15: Propagation Delay Comparison

VII. CONCLUSION

Handling sub threshold leakage power is a serious challenge in scaling of VLSI design technology in nano meter regime. We have introduced a power gating architecture with Multi-Threshold CMOS (MTCMOS) technique that provides multiple power-off modes which offers advantage of simplicity and less power. We have proposed and analyzed power gating architectures with efficient methodologies such as dual stack and body biasing to tackle leakage problem. Extensive simulation results are displayed and comparisons are done between recent power gating scheme and proposed schemes. The body biasing technique shows improved results in terms of optimizing low power and delay with reconfigurable architectures.

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