Cascaded Multilevel Inverter Fed Induction Motor Drive
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Abstract— In this paper instead of a classical multilevel inverter, a hybrid multilevel inverter is proposed to drive three phase induction motors. The proposed topology includes a three-phase inverter supplied by a DC voltage and three single-phase H-bridge inverters each supplied by separate DC sources. To maximize the output voltage levels of the hybrid multilevel inverter, the voltage of the single-phase inverters is half of the value of the three phase bridge inverter DC source [1][2]. In SPWM, POD technique is used to generate the gate pulses. A three phase induction motor is connected as load and its performance characteristics are analysed. Simulations have been carried out in MATLAB–Simulink R2013a (8.1.0.604) to study the performance of the proposed prototype.
Key words: H-bridge inverters, POD, MATLAB–Simulink

I. INTRODUCTION
The multilevel inverter has gained much attention in recent years due to its advantages in high power with low harmonics applications and higher voltage capability. Multilevel level inverter is an electronic circuit which converts input DC voltage to AC stepped output voltage so as to get an approximate sine wave. It is used for medium voltage high power applications such as utility system for controlling reactive power, hybrid electric vehicles etc. Three different major multilevel inverter structures have been applied in industrial applications cascaded H-bridges inverter with separate DC sources, diode clamped, and flying capacitors [5]. Including these three basic multilevel inverter topologies, other multilevel inverter topologies have been proposed [7]. The THD will be decreased by increasing the number of levels. It is obvious that an output voltage with low THD is desirable, but increasing the number of levels needs more hardware, also the control will be more complicated. Fig. 1, shows single phase topology of the Diode Clamped, Flying Capacitor, Cascaded H-bridge and Cascade Hybrid multilevel inverter and the components required by them is as shown in Table I.

<table>
<thead>
<tr>
<th>Types of multilevel inverter</th>
<th>Number of switches</th>
<th>Number of Diodes</th>
<th>Number of Capacitors</th>
</tr>
</thead>
<tbody>
<tr>
<td>Diode Clamped</td>
<td>8</td>
<td>12</td>
<td>4</td>
</tr>
<tr>
<td>Flying Capacitor</td>
<td>8</td>
<td>-</td>
<td>10</td>
</tr>
<tr>
<td>Cascaded H-bridge</td>
<td>8</td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td>Cascaded Hybrid</td>
<td>6</td>
<td>-</td>
<td>2</td>
</tr>
</tbody>
</table>

Table 1: Components Required For Different Topologies Of Five Level Single Phases Multilevel Inverter.

II. OPERATING PRINCIPLE OF THE FIVE LEVEL HYBRID CASCADe MULTILEvel INVERTER.
The topology of the proposed three phase five level cascaded hybrid multilevel inverter is shown in Fig. 2. The single phase topology of the hybrid multilevel inverter is shown in Fig. 3. The bottom bridge is single leg of a standard three leg three phase inverter which is supplied by DC source of Vdc and the top bridge is a full bridge inverter (H-bridge) which is in series with standard inverter leg that the H-bridge inverter is supplied by DC power source of Vdc/2; [3][4]. Considering the output voltage V1 of this leg is either +Vdc/2 when S1 closed or -Vdc/2 when S1 closed and the output voltage V2 of the H-bridge inverter is either +Vdc/2 when Sa1 & Sa3 closed, 0 when Sa1 & Sa3 or Sa2 & Sa4 closed, or -Vdc/2 when Sa2 & Sa3 closed. When the output voltage Vout = V1 + V2 is required to be zero, one can either set V1 = +Vdc/2 and V2 = -Vdc/2 or V1 = -Vdc/2 and V2 = +Vdc/2. In this flexibility switches are selected as per the required voltage.

Fig. 2: Three Phase Five Level Hybrid Cascaded Multilevel Inverter
Fig. 3: Single Phase Five Level Hybrids Cascaded Multilevel Inverter

In order to generate the PWM signal, the sinusoidal signal and the triangular signal is compared which is shown in Fig.4.[1] and the output of the PWM signal is either ‘1’ when \( V_{\text{cut}}>V_{\text{tri}} \) or ‘0’ when \( V_{\text{cut}}<V_{\text{tri}} \). During the circuit operation low switching losses is required, so three leg three phase inverter will operate on square wave mode and H-bridge inverter will operate on SPWM mode as shown in Fig.5.

Fig. 4: The Sinusoidal Reference Signal And The Triangular Signal To Generate PWM Pulses

Fig. 5: Output Waveform Of The Single Phase Five Level Hybrid Cascaded Multilevel Inverter

Fig. 6: SPWM Technique to Generate Pulses To H-Bridge.

III. THREE PHASE INDUCTION MOTOR

A three phase asynchronous motor is connected to the proposed circuit to evaluate its performance characteristics whose equivalent circuit for single phase of the rotor is shown in Fig. 7; [6][7] and motor parameters are shown in below table II. Because of the open loop, speed of rotor varies between 155 rad/sec to 160 rad/sec as per the results of speed-time curve. To verify the validity of the proposed five level hybrid multilevel inverter fed induction motor drive the results of both output voltage and FFT analysis are verified by simulating the main circuit using MATLAB-Simulink R2013a (8.1.0.604).

Fig. 7: Equivalent Circuit Refer To Stator.

Rotor current is

\[
I_r = \frac{s E_r}{(R_r + jX_r)} \tag{3}
\]

Table II: Induction Motor Parameters

<table>
<thead>
<tr>
<th>Nominal Power</th>
<th>3750W</th>
</tr>
</thead>
<tbody>
<tr>
<td>Voltage (line-line)</td>
<td>460V</td>
</tr>
<tr>
<td>Frequency</td>
<td>50Hz</td>
</tr>
<tr>
<td>Poles</td>
<td>4</td>
</tr>
<tr>
<td>Stator Resistance</td>
<td>1.115ohm</td>
</tr>
<tr>
<td>Stator Inductance</td>
<td>0.005974ohm</td>
</tr>
<tr>
<td>Rotor Resistance</td>
<td>1.083ohm</td>
</tr>
<tr>
<td>Rotor Inductance</td>
<td>0.005974ohm</td>
</tr>
<tr>
<td>Mutual Inductance</td>
<td>0.2037ohm</td>
</tr>
</tbody>
</table>

The frequency modulation \( m_f = f_c/f_m \) is defined as

\[
m_f = \frac{f_c}{f_m} \tag{1}
\]

The amplitude modulation \( m_a = A_m/A_c \) is defined as

\[
m_a = \frac{A_m}{A_c} \tag{2}
\]
Fig. 8: Simulink Model To Generate Gating Pulses For H-Bridge.

Fig. 9: Single Phase Five Level Inverter Output Voltage.

Fig. 10: Proposed Three Phase Five Level Hybrid Cascaded Multilevel Inverter.

Fig. 11: Three Phase Five Level Inverter Output Voltages.

Fig. 12: Rotor Currents of Asynchronous Motor.

Fig. 13: Stator Currents Of Asynchronous Motor.

Fig. 14: Speed and Torque Curve With Respect To Time.

Fig. 15: FFT Analysis.
V. CONCLUSION

Five level three phase hybrid cascaded multilevel inverter consists of a standard three phase inverter and three H-bridge inverters with DC sources of 200V and 400V. In SPWM, POD technique is used to generate the pulses with sinusoidal reference signal frequency 50Hz and carrier signal frequency 2000Hz. Performance characteristics of the three phase induction motor is found to be satisfactory by connecting it to proposed circuit. For the proposed Multilevel Inverter fed Induction Motor THD value of output voltage is found to be 3.95.

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REFERENCES