Low Power Pulse Triggered Flip Flop with Modified Conditional Pulse Enhancement Scheme

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Abstract— In this work, a low-power pulse-triggered flip-flop (FF) with modified conditional pulse enhancement scheme is proposed. The proposed design fulfills the discharging problem using the pulse generation control logic, an AND function, which facilitates a faster discharge operation. A two-transistor AND gate design is used to reduce the circuit complexity and modified conditional pulse-enhancement technique is devised to speed up the discharge along the critical path when circuit required. Modified scheme is used different approach to provide delay in the CLK. As a result, transistor sizes in pulse-generation circuit and delay inverter can be reduced for power saving. All simulation results are based on using CMOS 90-nm process technology at 500MHz clock frequency. Its maximum power saving against conditional pulse FF is up to 8.85%.

Key words: Flip-Flop, Low Power, Pulse-Triggered FF

I. INTRODUCTION

Flip flops are used as the main storage elements in most of the digital devices such as register files, FIFO, counters and shift registers. It is estimated that the power consumption of the clock system, which consists of clock spreading networks and storage elements, is as high as 48-50% of the total system power. FFs contribute a large portion of the chip area and power consumption to the overall system design. Pulse-triggered FF (P-FF) is more popular than the conventional transmission gate (TG) and master–slave predicated FFs in high-speed applications because of its single-latch structure. Besides the speed advantage, its circuit simplicity lowers the power consumption of the clock tree system. A P-FF consists of a pulse used for strobe signals and a latch used for data storage. If the triggering pulses are very narrow, then latch acts like an edge-triggered FF. Since only one latch is needed for a P-FF than two used in the conventional master–slave configuration. This leads to a higher toggle rate for high-speed operations. P-FFs withal sanction time borrowing across clock cycle boundaries and feature a zero or even negative setup time. Regardless of these advantages, pulse generation circuit requires delicate pulse width control to deal effective with possible variations in process technology and signal distribution network. In this, a statistical design framework is developed to take these factors into account. To obtain better performance among delay, power and area, design space exploration is withal a widely used technique.

In this paper, we have presented a low-power pulse-triggered FF design with modified conditional pulse enhancement scheme. In the second section, we present the previous pulse-triggered flip-flop with pulse enhancement scheme. In the third section, we present the proposed flip-flop with description. In the fourth section, we show the simulation results with comparison table. And in last section, we conclude the results.

II. CONVENTIONAL FLIP-FLOP

The conventional pulse-triggered flip-flop (PT-FF) with pulse enhancement scheme [1] is shown in the Fig.1. Three additional transistors are employed to support this feature. Total transistors of the pulse generation logic benefit from significant size reductions and the overall layout area is even slightly reduced. This gives hike to competitive power and power–delay–product performances against other P-FF designs.

In this design, the longest discharging path is formed when input data is "1" while the Qbar output is "1." To enhance the discharging under this condition, an extra transistor P3 is added at the top. This transistor is normally turned off because node X is pulled high most of the time. After the rising edge of the clock, the clock delay inverter drives output node back to zero but with little delay. This generates the clock pulse and the generated clock pulse is taller in height, which enhances the pull-down strength of lower N6 transistor which is responsible for the discharging. After the clock has reached to logic 1, then lower N6 is turn off due to no clock pulse. Then voltage level of node X rises and turns off upper P3 transistor eventually.

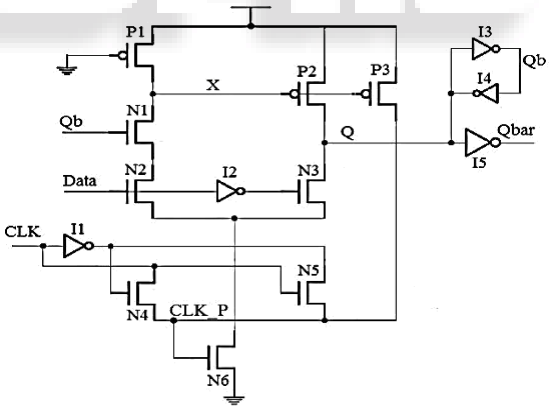


Fig. 1: A Pulse-Triggered Flip Flop with Conditional Pulse Enhancement Scheme

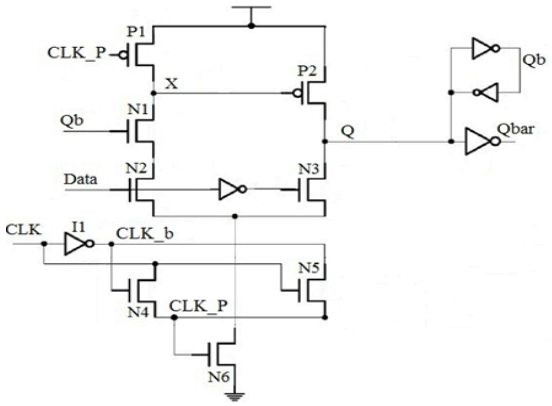
With the help of extra P3 transistor, the width of the generated discharging pulse is stretched out. This creates a pulse with sufficient width for correct data requirement, a bulky delay inverter design, which comprises most of the power consumption in pulse generation logic, is no longer required. It should be noted that this conditional pulse enhancement technique takes effects only when the FF output is subject to a data change from 0 to 1. The leads to a low power consumption than those schemes using an indiscriminate pulsewidth enhancement approach. Another advantage of this conditional pulse enhancement scheme is the reduction in leakage power due to shrunken transistors in the critical discharging path and in the delay inverter.

III. PROPOSED WORK

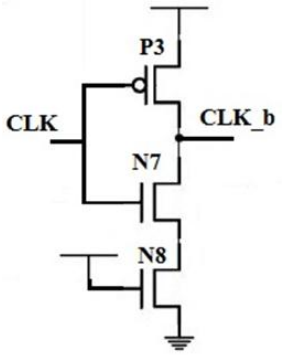
Proposed FF is shown in Fig. 2(a). New FF design, with the new clock pulse generator which has the modified conditional pulse with enhancement scheme, is described below. In this clock pulse generator, two pass transistors are used as a AND gate to generate a clock pulse (CLK_P) at the rising edge of the clock signal that drive transistor N6 which is responsible for the discharging operation. In Fig. 2(b), Inverter I1 is designed in such a way that delay is created in CLK_b due to extra transistor N8 at the rising edge of the CLK. It provides better CLK_P (in height and width) than the previous FF CLK_P. So it reduces the power consumption and delay in the proposed flip-flop. In the previous design, transistor P1 is always ON due to ground applied at the gate terminal. So, it dissipates more power during the switching of the node X. But in new design, transistor P1 is almost OFF during the discharging of the node X that lowers the power dissipation in the FF.

III. SIMULATION RESULTS

Conventional FF is described in section II and proposed FF is explained in section III. All simulations have carried out at 90nm process technology, 1V power supply and 500MHz clock frequency with the 100 % switching activity of the Data with respect to CLK. A 15fF capacitor has been loaded at the output of the FFs. Comparison of the both FFs are shown in Table I which contains the power dissipation at 100% switching activity, Data-to-Q delay, no. of transistors and power-delay product (PDP). Simulation waveforms are shown in Fig. 3.



(a)



(b)

Fig. 2: (a) Pulse-triggered FF design with modified conditional pulse enhancement scheme (b) Design of inverter I1 used in clock pulse generation circuit.

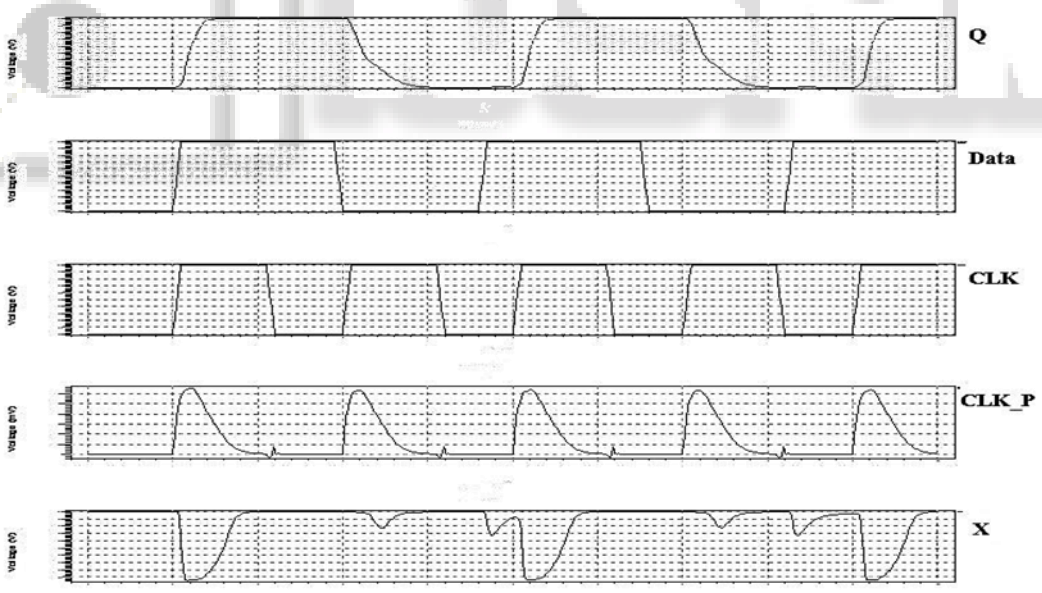


Fig. 3: Output Waveforms of Proposed Flip Flop

S. No.	Flip Flop	No. of Transistors	Power (uW)	Delay (ps)	PDP (fJ)
1	PT-FF with pulse enhancement scheme	19	25.18	148.45	3.73
2	Proposed FF with modified pulse enhancement scheme	19	19.15	124.53	2.38

Table I. Comparison of conventional and proposed flip flops

IV. CONCLUSION

In this paper, we devise a low-power pulse-triggered FF design with modified conditional pulse enhancement scheme by employing one new design measures. This successfully reduces the number of transistors stacked along the discharging path using a PTL-based AND logic with one transistor supports conditional enhancement to the height

and width of the discharging pulse so that the size of the transistors in the pulse generation circuit can be kept minimum. Proposed design has maximum power saving against conditional pulse FF up to 8.85%.

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