VHDL Implementation of HD 15530

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Abstract— 'Manchester coding' is a Digital Line coding technique. It is used in areas like Bio-medical applications, Magnetic recordings, Satellite Communication, Servo systems, and various industrial applications. Manchester coder and decoder implementation is described in this paper. The Intersil HD-15530 is a high performance CMOS device IC. It is intended to service the requirements of military standard MlL-STD-1553 and time division multiplexed serial data protocols. The LSI chip has two sections, an Encoder and a Decoder. The encoder and decoder sections can operate completely independent of each other, except for Master Reset functions. The Encoders function is to produce the sync pulse, the parity bit as well as encode the data bits. The Decoders function is to recognize the sync pulse, identify it, decode the data bits and check parity. This IC supports 1MHz data rate of military standard MlL-STD-1553. This system is implemented in VHDL language using ModelSim Software for simulation.

Key words: Manchester Coding, HD-15530, MlL-STD-1553

I. INTRODUCTION

Manchester coding technique is a digital line coding technique in which all bits of the binary data are arranged in a particular sequence. Here a bit '1' is represented by transmitting a high voltage for half duration of the input signal and an inverted signal for the next halftime period. When transmitting '0' in Manchester format, a low voltage will be send for the first half cycle, and a high voltage is send for the next half cycle. When a data having continuous high signals or continuous low signal is sending, it is difficult to calculate the number of 1s and 0s in the data as there is no transition from low to high or high to low for a particular time period. The detection is possible by calculating the time duration of the signal. But when the signal is coded in Manchester format there will be always a transition from high to low or low to high for each bit. Thus for a receiver it is easier to detect the data in Manchester format. The probability for occurrence of an error is very low in Manchester format and it is a universally accepted digital encoding technique.

The Intersil HD-15530 is a high performance CMOS device. It is intended to service the requirements of MlL-STD-1553 and similar Manchester II encoded, time division multiplexed serial data protocols. This LSI chip has two sections, an Encoder and a Decoder. These sections can operate completely independent of each other, except for the Master Reset functions. The Encoder produces the sync pulse, the parity bit as well as encode the data bits. The Decoder recognizes the sync pulse, identifies it as well as decode the data bits and check parity. This integrated circuit is fully guaranteed to support the 1MHz data rate of the military standard MlL-STD-1553 over both temperature and voltage. It interfaces with CMOS, TTL or N channel support circuitry. It uses a standard 5V supply.

II. LITERATURE REVIEW

A. VHDL implementation of Manchester encoder and decoder [5]

An implementation of Manchester coding is described in this paper. Manchester coding technique is a digital line coding technique in which all the bits of the binary data are arranged in a particular sequence. The Intersil HD-15530 is a high performance CMOS device which is intended to service the requirements of MlL-STD-1553 and similar Manchester II encoded, time division multiplexed serial data protocols. Here, Manchester encoding and decoding operations are achieved by VHDL coding language. All the codes are written with reference to IC HD15530, CMOS Manchester encoder and decoder. HD15530 IC contains a Manchester encoder and decoder blocks. These sections can operate independent of each other, except for the Master Reset functions. This circuit meets many of the requirements of the databus MIL-STD- 1553.

B. Design of 16 Bit UART based on VHDL [3]

This paper describes the design of UART based on VHDL language. Serial transmission technique is used in transmitting a bit in UART. UART is considered as a low speed, low cost data exchange between computer and peripherals. To overcome this problem of low speed data transmission, a 16 bit UART is proposed in this paper. It works on 9600bps baud rate. This will result in increased speed of UART. Whole design is simulated using Xilinx ISE8.2i software and results are completely consistent with UART protocol. Here VHDL is used as the programming language.

C. Manchester Encoder and Decoder [2]

To make the transmitting data robust, efficient and accurate some encoding and decoding techniques are used in communication. One such coding technique is 'Manchester coding' which comes under Digital Line Encoding and Decoding techniques that are widely used in Industrial applications. To avoid the DC term in the transmitting signal, Manchester coding is used which always makes a transition at the middle of each bit. This paper deals with the implementation of a Manchester Encoder and Decoder circuit, along with invalid detection and clock recovery unit (CRU) using HDL (Hardware Description Language). Here the programming of the Manchester Encoder and Decoder is done using Verilog Hardware Description Language and the simulation is done using ModelSim 6.4SE software.

D. MIL-STD-1553 bus controller terminal [1]

In this paper introduction to the MIL-STD-1553 data bus, its history, working, applications and use is studied. This paper describes the physical elements that make up the bus, the protocol, including the message formats, word types, and command and status words of MIL-STD-1553 Data bus,

implementation of MIL-STD-1553 Bus Controller terminal. Its information transfer formats is coded using ModelSim.

E. VHDL implementation of a telemetry system [4]

In this paper, it is proposed to design a telemetry system using VHDL. The telemetry, tracking and command (TT&C) system of a spacecraft provides the most important telecommunication link between a satellite and ground station. Here Manchester coding technique and Binary Frequency Shift Keying Modulation technique has been used for the design purpose. Transmitter and receiver section of a telemetry system is designed using VHDL code in this project. The code is synthesized and simulated using ISE Xilinx software.

III. DESIGN OVERVIEW

In this project, the Manchester encoding and decoding operations of IC HD-15530 are achieved by using VHDL coding technique. The Intersil HD-15530 is a high performance CMOS device which is intended to service the requirements of MlL-STD-1553. The encoder and decoder sections can operate completely independent of each other, except for the Master Reset functions.

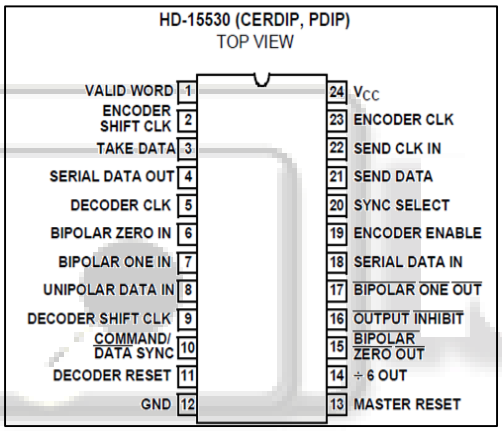

Fig. 1: Pin diagram of IC HD-15530

A. Manchester Encoder

1) Block Diagram

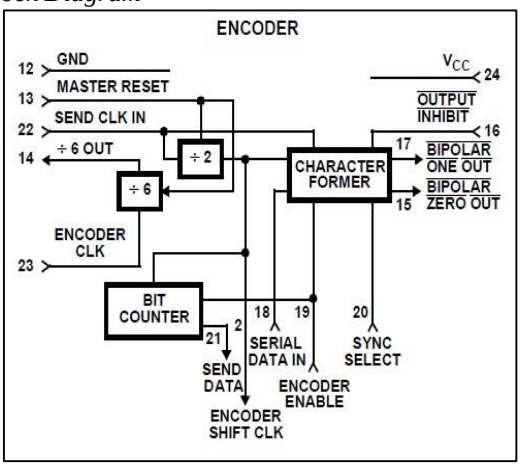

Fig. 2: Block diagram of Manchester encoder

The block diagram of Manchester encoder implemented with reference to HD-15530 is as shown above.

2) Encoder Operation

The Encoder requires a single clock with frequency twice the desired data rate applied at the SEND CLOCK input. An auxiliary divide by six counter is provided on chip which is utilized to produce the SEND CLOCK by dividing the DECODER CLOCK.

When ENCODER ENABLE is high during a falling edge of ENCODER SHIFT CLOCK, the Encoder's cycle begins. Encoder cycle lasts for one word length or twenty ENCODER SHIFT CLOCK periods. At the next low-to-high transition of the ENCODER SHIFT CLOCK, a high on SYNC SELECT input actuates a command sync or a low will produce a data sync for the word. When the Encoder is ready to accept data, the SEND DATA output will go high and it remains high for sixteen ENCODER SHIFT CLOCK periods. During these sixteen periods the data will be clocked into the SERIAL DATA input with every high-to-low transition of the ENCODER SHIFT CLOCK and it will be sampled on the low-to-high transition. After the sync and Manchester II coded data are transmitted through the BIPOLAR ONE and BIPOLAR ZERO outputs, the Encoder adds on an additional bit which is the parity bit for that word. If ENCODER ENABLE is held high continuously, then consecutive words will be encoded without an interframe gap.

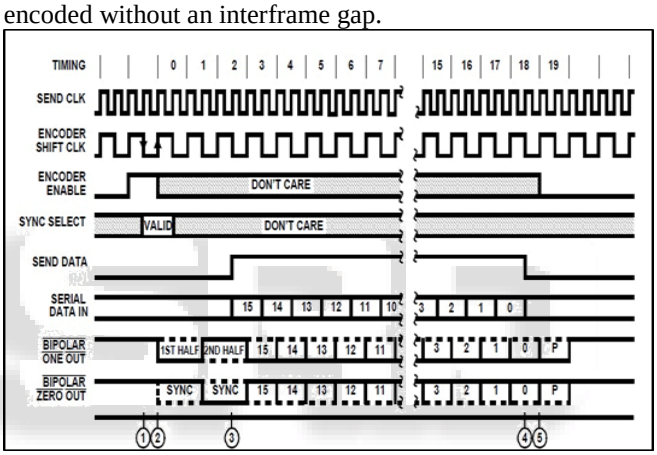

Fig. 3: Timing diagram of Manchester encoder

So ENCODER ENABLE must go low by time to prevent a consecutive word from being encoded. At any time a low on OUTPUT INHIBIT input will force both the bipolar outputs to a high state but it will not affect the Encoder in any other way. To abort the Encoder transmission, a positive pulse must be applied at MASTER RESET input. Any time after or during this pulse, a rising edge of SEND CLOCK clears the internal counters and initializes the Encoder for a new word.

B. Manchester Decoder

1) Block diagram

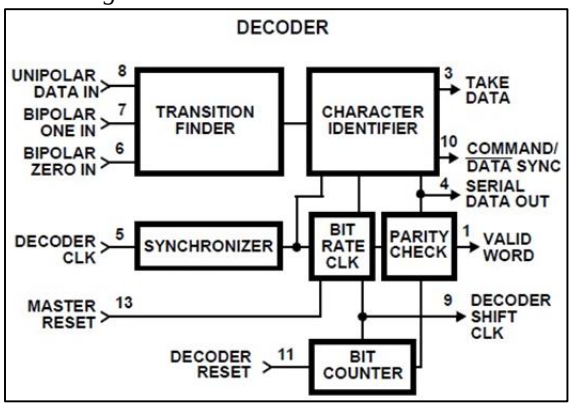

Fig. 4: Block diagram of Manchester decoder

The block diagram of Manchester decoder implemented with reference to HD-15530 is as shown below:

2) Decoder operation

The Decoder requires a single clock with a frequency of 12 times the desired data rate applied at the DECODER CLOCK input. The Manchester II coded data can be presented to the Decoder in one of two ways. The BIPOLAR ONE and BIPOLAR ZERO inputs will accept data from a comparator sensed transformer coupled bus as specified in Military Spec 1553. The UNIPOLAR DATA input can only accept non-inverted Manchester II coded data. (e.g. from BIPOLAR ONE OUT of an Encoder through an inverter to Unipolar Data Input).

The Decoder is free running and continuously monitors its data input lines for a valid sync character and two valid Manchester data bits to start an output cycle. When a valid sync is recognized, the type of sync is indicated on COMMAND/DATA SYNC output. If the sync character was a command sync, this output will go high and remain high for sixteen DECODER SHIFT CLOCK periods, otherwise it will remain low. The TAKE DATA output will go high and remain high - while the Decoder is transmitting the decoded data through SERIAL DATA OUT. The decoded data available at SERIAL DATA OUT is in NRZ format. The DECODER SHIFT CLOCK is provided so that the decoded bits can be shifted into an external register on every low-to-high transition of this clock. Note that DECODER SHIFT CLOCK may adjust its phase up until the time that TAKE DATA goes high. After all sixteen decoded bits have been transmitted the data is checked for odd parity. A high on VALID WORD output indicates a successful reception of a word without any Manchester or parity errors. At this time the Decoder is looking for a new sync character to start another output sequence. VALID WORD will go low approximately 20

DECODER SHIFT CLOCK periods after it goes high if not reset low sooner by a valid sync and two valid Manchester bits as shown.

At any time in the above sequence a high input on DECODER RESET during a low-to-high transition of DECODER SHIFT CLOCK will abort transmission and initialize the Decoder to start looking for a new sync character.

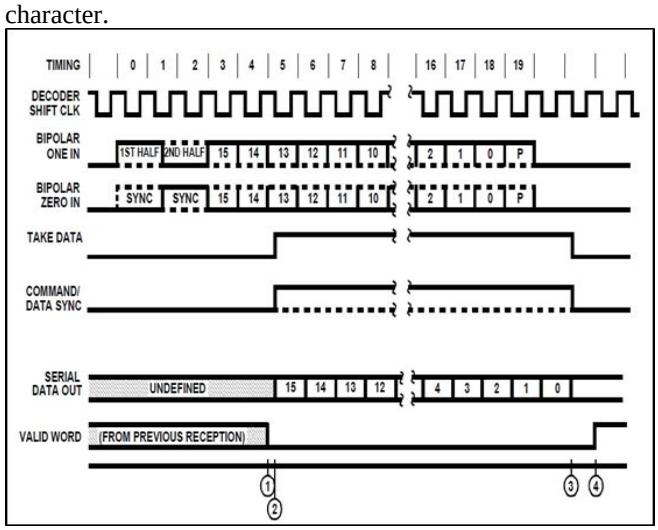

Fig. 5: Timing diagram of Manchester decoder

IV. PROGRAMMING AND SIMULATION

This system was realized in VHDL language using MODEL SIM Software. VHDL is an acronym for Very High Speed Integrated Circuits Hardware Description Language. It is a hardware description language that can be used to model a digital system. A hardware description of the digital system is called an entity. An entity X when used in another entity becomes a component for the entity Y. Therefore a component is also an entity, depending on the level at which we are trying to model.

A digital system can be represented at different levels of abstraction. The highest level of abstraction is the behavioral level that describes a system in terms of what it does or how it behaves. A behavioral description specifies the relationship between the input and output signals. The structural level, on the other hand, describes a system as a collection of gates and components that are interconnected to perform a desired function. It is a representation that is usually closer to the physical realization of a system. VHDL allows one to describe a digital system at the structural or the behavioral level. The behavioral level can be further divided into two kinds of styles: Data flow and Algorithmic. The dataflow representation describes how data moves through the system. The data flow model makes use of concurrent statements that are executed in parallel as soon as data arrives at the input. On the other hand, sequential statements are executed in the sequence that they are specified. VHDL allows both concurrent and sequential signal assignments that will determine the manner in which they are executed.

Once an entity is modeled it needs to be validated by a VHDL system. Once the sample circuit is completed design is to be simulated to verify that it actually does what it is intended to do. Test benches apply some sequence of inputs to the circuit being tested (the unit under test, or UUT) so that its operation can be observed in simulation. A test bench must consist of a component declaration corresponding to the UUT, and a description of input stimulus being applied to the UUT. Thus the test bench can be defined as virtual environment which is used to verify the correctness or soundness of the hardware model.

ModelSim is a verification and simulation tool for VHDL, Verilog, System Verilog, and mixed language designs. Mentor Graphics was the first to combine single kernel simulator (SKS) technology with a unified debug environment for Verilog, VHDL, and System C.

In ModelSim, all designs are compiled into a library. A new simulation in ModelSim is started by creating a working library called "work". "Work" is the library name used by the compiler as the default destination for compiled design units. After creating the working library, compile the design units into it. The ModelSim library format is compatible across all supported platforms. The design can be simulated on any platform without having to recompile the design. With the design compiled, load the simulator with the design by invoking the simulator on a top-level module (Verilog) or a configuration or entity/architecture pair (VHDL).

Assuming the design loads successfully, the simulation time is set to zero, and enter a run command to begin simulation. If the expected results are not getting, ModelSim's robust debugging environment can be used to

track down the cause of the problem. The Wave window allows you to view the results of your simulation as HDL waveforms and their values.

V. CONCLUSION

This project describes the "VHDL Implementation of Manchester Encoder and Decoder". It gives an easy and less expensive way to implement Manchester coding system. First the different components that constitute the encoder and decoder have been designed with required inputs, outputs & control signals. The interface between the designed components has been formulated. This was then realized in VHDL language using ModelSim Software. In ModelSim, all designs are compiled into a library. The design was thoroughly simulated to test all the instructions in VHDL simulator software. As the coding system has high accuracy, the system gives more accuracy and efficiency in data sending.

VI. APPLICATIONS

Data bus standards are inevitable in all electronic systems. MIL-STD-1553 is a data bus standard which is mainly used in military avionics applications for data transfer between critical systems in an aircraft.

A. Military Aerospace

Military aircrafts utilize MIL-STD-1553 data buses, which allow complex electronic subsystems to interact with each other and the on-board flight computer.

B. Space Applications

DSCC Class "K" certified MIL-STD-1553 data buses are used to form a common data link between space applications. It has been designed into the following space applications such as The International Spaces Station, Advanced Extremely High Frequency (AEHF) Satellite

C. Commercial Aerospace

Historically the commercial avionics designers have preferred other data bus protocols for their systems, but are now finding that MIL-STD-1553 fits the needs in newer systems.

D. Weapon Systems

The MIL-STD-1553 data buses are heavily used in weapon systems like Military missiles and smart bombs to download information from the aircraft to launch and coordinate information during the flight of the weapon.

E. Ground Vehicles

Military ground vehicles use MIL-STD-1553 data buses to form the data links between electrical subsystems. It has become highly technical and sophisticated mechanisms.

VII. FUTURE SCOPE

The data bus technologies such as IEEE1394B Fire wire, Fiber Channel, and GbE are higher-performance data buses which are moving into areas which are only occupied by MIL-STD-1553. Today's modern aircraft use a mix of such high-performance data buses and 1553. These new technologies bring higher network speeds than MIL-STD-1553 which offers a 1Mbps speed and are well suited for applications such as video transmission and sensor displays where high bandwidth is required.

A. New High Speed 1553

Existing aircraft requires a higher speed. But it is very costly to Re-wire on an existing system. The Time on Ground to re-wire existing aircraft is also prohibited. A solution for this can be the New High Speed 1553 that works with existing wiring efficiently.

REFERENCES

[1] Ancy Das. A. S, Aravindhan. A, "MIL-STD-1553 bus controller terminal," International Journal of Computer Engineering & Science, Vol. 4, Issue. 2, pp. 1-12, March 2014
[2] Anjali. V, P. Satishkumar, "Manchester Encoder and Decoder with Clock Recovery Unit and Invalid Detector," Computer Engineering and Intelligent Systems, Vol. 6, Issue. 2, pp. 18-22, 2015
[3] Bit UART Serial Communication Module Based on VHDL," International Journal of Emerging Technology and Advanced Engineering, Vol. 4, Issue. 4, pp. 20-26 ,April 2014
[4] P. K. Dakua1, P.K Nanda, "Design of telemetry system using VHDL," International Journal of Recent Scientific Research, Vol. 5, Issue. 12, pp. 2295-2297, December 2014
[5] Suchitra Suresh, "VHDL implementation of Manchester encoder and Decoder," International Journal of Electrical, Electronics and Data Communication, Vol. 1, Issue. 2, pp. 43-47, April 2013
[6] Technical papers from VSSC library

