Realization of FPGA based Data Acquisition System using Soft Core Embedded Processor and Network Module

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Abstract— This paper presents novel approach to the design and implementation of data acquisition board consisting of FPGA, ADC and Ethernet Controller module (WIZ-830MJ). The board converts analog signal into digital data and transmits the remote results through Ethernet interface. Board contains two interface out of which SPI interface deals with communication between ADC and FPGA and Ethernet interface deals with communication between DAQ board and host PC. The processor implemented on FPGA works as TCP Server which allows communication of data through client-server session. The control signal for interfacing ADC and Network Module is generated in FPGA. Xilinx ISE is used to write VHDL Code in FPGA. The LabVIEW program is used to display the acquired data.

Key words: ADC, DAQ, FPGA, Ethernet, LabVIEW

I. INTRODUCTION

Data Acquisition is the process of sampling signals and converting the resulting samples into digital numeric values that can be manipulated by computer. In general, data acquisition system typically converts analog waveforms into digital values for processing. For the purpose monitoring the signals in real time, the data is transferred to host through various interfacing standards such as RS232, USB, CAN bus, PCI, Ethernet etc. Out of these several options available, Ethernet is now-a-days widely used option as it has much faster speed, has better shielding against magnetic disturbance, can go upto long distance etc. The aim is to design and implement data acquisition system using Ethernet controller. Hence the fully integrated system in FPGA composed of two main parts: acquisition and processing of data part, and communication part that consists of architect of Micro-blaze processor which takes processed data and can transmit them by running libraries for TCP/IP communication. The model has an Ethernet interface which was used for remote communication[3].

The objective of this work is the design and implementation of DAS in which data is fetched through ADC and those data are fed to Micro-blaze (MCS) i.e. embedded processor. The data from MCS is passed to network module and are then feed to host PC through Ethernet. The organization of this paper is as follows: Section II gives block diagram and brief overview of main components, Section III gives implementation details, Section IV describes testing and results, Section V concludes the work.

II. BLOCK DIAGRAM

Block Diagram of implemented system is as shown in Fig 1. Signals coming from sensors can be taken as analog input of ADC and corresponding 24 bit digital data is obtained. Here ADS1278 works in high resolution mode. The digital data obtained from ADC is fed to Micro-blaze Processor.

The data from MCS data bus is shared to WIZ-830MJ and then it is transferred to host PC through Ethernet.

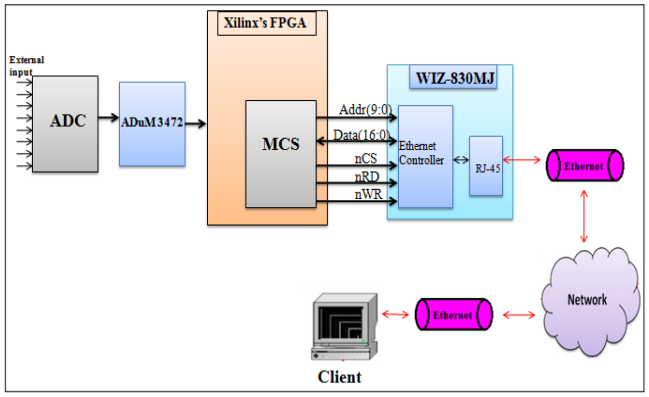

Fig. 1: Block Diagram

A. ADS1278

The ADS1278 is 24 bit delta sigma analog to digital converter allowing simultaneous sampling of eight channels. Here ADS1278 is made to operate in high resolution mode giving data rate upto 52ksps and SNR of 111 db. The data is retrieved in SPI format (i.e. data will be further transferred to FPGA serially).

B. ADuM3472

[12]The ADuM3472 is quad-channel, digital isolators with an integrated PWM controller and transformer driver for an isolated dc-to-dc converter. This eliminates the need for a separate, isolated dc-to-dc converter in 2W isolated designs. The ADuM3472 isolator provides four independent isolation channels in a variety of channel configurations and data rates.

C. SPARTAN-6

The Xilinx make SPARTAN-6 family's Field Programmable Gate Array (FPGA) is used here as a main processing and logic core, since they offer system flexibility and reconfiguration. Also as present FPGAs incorporate high-speed interfaces, soft microprocessor, which make it more flexible by making it capable of featuring sequential programming too. The Spartan-6 family offers high-volume system designers with multiple advantages that are not found in alternative products such as small form factor, high speed I/O, power down modes etc.

D. MCS

Micro blaze is 32 bit soft processor that is a part of embedded development kit designed for Xilinx's FPGA. The designing of system is implemented by writing logic for ADC and Ethernet controller in SDK software application to run on Micro blaze processor. C/C++ language can be used

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for developing software application. Software application controls the functionality of IP Core added to processor.

E. WIZ-830MJ

It is a network module that supports 8 independent sockets simultaneously and has 16/8 data bus width. It includes hardware Ethernet/internet protocols and can give high network performance upto 50Mbps.

III. IMPLEMENTATION DETAILS

A. SPI Interface

It was used for communication between ADS1278 and FPGA. Interfacing diagram is shown in Fig 2. The control signals for ADC i.e. SCLK, SYNC and DRDY are generated by FPGA. ADC is used in TDM mode and data is retrieved in SPI format. Hence the data is transferred from ADC to FPGA serially.

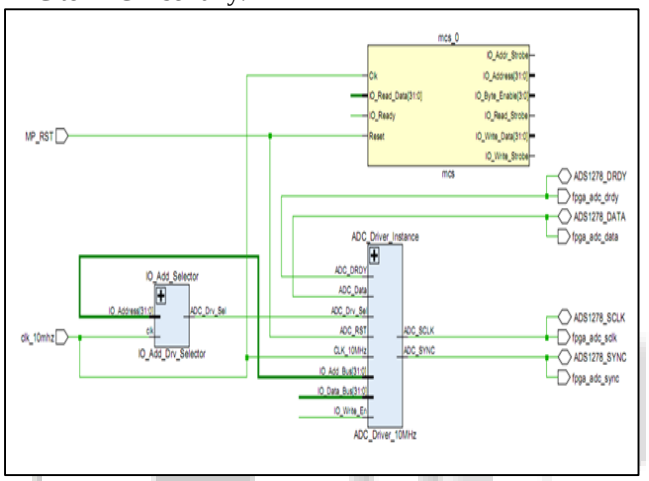

Fig. 2: RTL Schematic of interfacing of MCS and ADC

Total 96 bits of 4 channels are serially shifted. Timing diagram of ADC was observed on GPIO pins available on board which is shown in Fig 3.

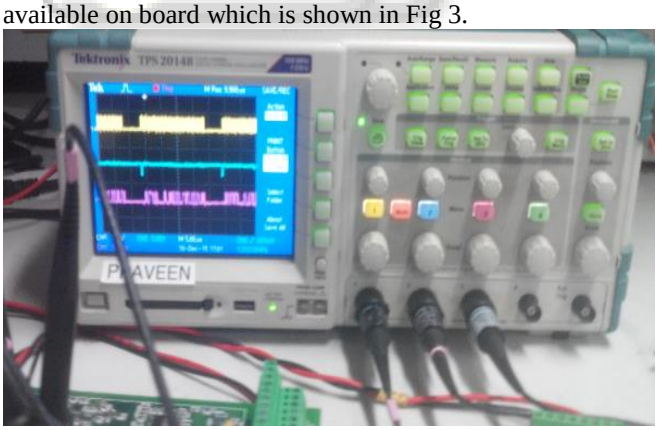

Fig. 3: Timing Diagram of ADC observed on Scope from GPIO pins available on board

B. Interfacing Between FPGA and WIZ-830MJ

Data Communication between FPGA and WIZ-830MJ was achieved through MCS. Interfacing diagram is as shown in Fig 4.

Networking functions is achieved by setting the register of network module through VHDL program written in Xilinx's FPGA. Xilinx's FPGA and WIZ-830MJ is used as server side of TCP protocol in hardware.

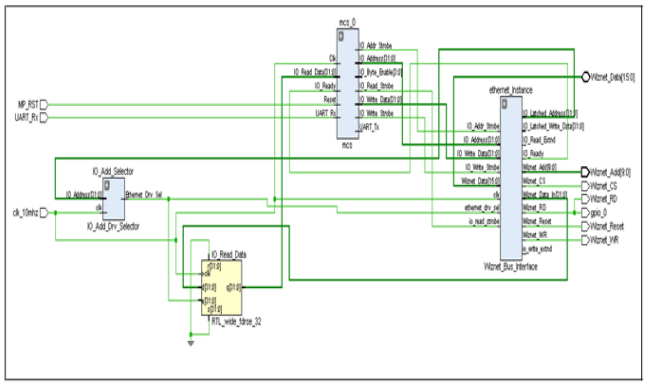

Fig. 4: RTL Schematic of interfacing of MCS and WIZ-830MJ

C. Data Communication

Modern FPGA has variety of communication options with host PC such as RS232, CAN, Ethernet etc. Out of this various interface standards, [4]Ethernet has proven to be effective and very economical PC networking solution. TCP protocol is widely used protocol for data communication as it has very important features.

FPGA and Network Module are used as server part of TCP protocol. Graphical user interface Screen is designed in LabVIEW which is used as client part of TCP protocol. Flow chart for the same is shown in Fig 5. Front Panel of Client part is shown in Fig 6. As a result of establishment of TCP/IP link between DAQ board and the host PC, the board should respond to the PING command having IP address allocated to board. The response of Pinging is shown in Fig 7.

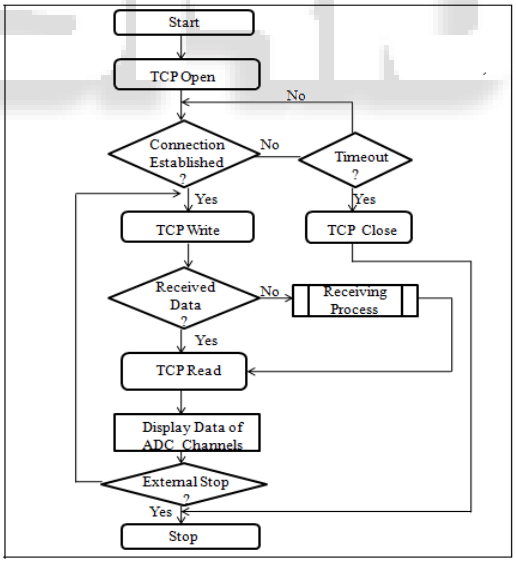

Fig. 5: Flow Chart

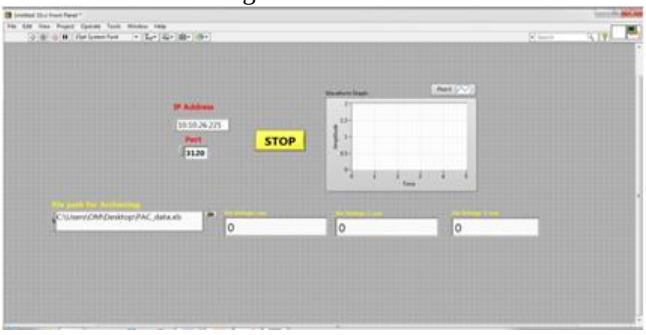

Fig. 6: Front panel of TCP Client

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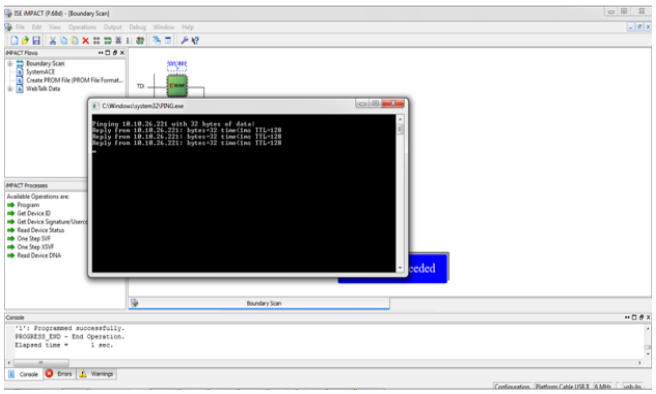

Fig. 7: Response given by network module to Ping Command

D. Software Description

1) Xilinx ISE Design Suite 14.6

All logic related to interfacing various modules such as ADC, WIZ-830MJ, FPGA, creation of TCP Server for the communication is done using VHDL on Xilinx ISE design tool. An embedded processor using Microblaze IP core has been created to serve all the control and communication purpose. All the required codes for Microblaze are developed in Xilinx Software development kit (SDK).

2) NI LabVIEW 2012:

LabVIEW (Laboratory Virtual Instrument Engineering Workbench) is created by National Instruments. LabVIEW programs are called Virtual Instruments. Application program in host PC is made using LabVIEW which act as a client part of TCP protocol.

IV. TESTING AND RESULTS

For purpose of testing only, counter was made in one of channel of ADC through VHDL Coding and external dc voltage was given in other two channels. Data from ADC is serially shifted in FPGA. MCS serves the purpose of communication between FPGA and WIZ-830MJ. Hence data from FPGA is transferred to WIZ-830MJ via MCS. Then data transmits to network via Ethernet.

Ramp Waveform was seen on front panel which is shown in Fig 8 as a result of counter made. This indicates successful transmission of data from server side to client side. It also indicates proper establishment of link between all the components.

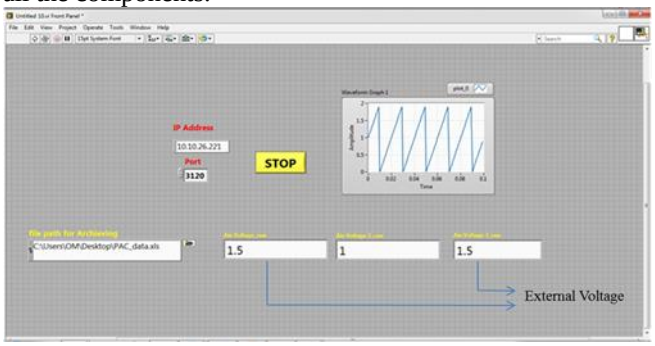

Fig. 8: Output on Front Panel of LabVIEW

V. CONCLUSIONS

In this paper, FPGA based platform is used to implement a data acquisition system as opposed to more traditional DSP platforms. Micro-Blaze Processor being used is soft core processor which has many advantages as compared to hard Processor. Also system uses Ethernet interface standards for data transmission from server to client which has several advantages as compared to other interface standards. Also by allowing parallel acquisition channels, there can be substantial improvement in speed of data acquisition. We have succeeded in establishing TCP/IP link between DAQ board and client GUI developed using LabVIEW with the help of Ethernet Controller. We are able to acquire external voltage and also can be monitored on Front Panel (client).

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