A Review on Reconfigurable Multisoft Core Architecture on FPGA

Pooja. H. Mane1 Pradeep C. Bhaskar2
1,2Department of Technology
1,2Shivaji University, Kolhapur (MS), India

Abstract—To achieve the high performance of multimedia applications, multiple processing units are required which are integrated into embedded systems. soft core processors and field programmable gate arrays (FPGAs) are a cheap and fast option to develop and test such systems. There are many platforms on which architecture is implemented, but still performance of the system is not that much of efficient. Reconfigurable platform is one of the best platforms for designing the new system.

Key words: Reconfigurable, Multisoft Core, Architecture

I. INTRODUCTION

A soft-core processor is hardware description language (HDL) model of specific processor (CPU) that can be customized for a given application and synthesized for an ASIC or FPGA target. Several advantages of soft core processors are easier to understand, designer can change the core by editing source code or selecting parameters.

Application specific integrated circuits are designed to perform a specific application. They perform very efficiently and fast while executing a given computation, also circuit cannot be modified after its fabrication, if any parts of the circuit requires modifications then it is necessary to redesign a chip.

Re-configurable computing is intended to fill the gap between hardware and software. Re-configurable devices, including field-programmable gate arrays (FPGAs), contain an array of computational elements whose functionality is determined through multiple Programmable configuration bits. These elements are known as logic blocks connected using programmable routing resources. In this way digital circuits can be mapped to the re-configurable hardware by computing the logic functions of the circuit within programmable logic blocks, logic blocks are connected together to form a network.

Parallel programming and parallel system on chip (SoC) such as multiprocessor systems are proposed. Embedded systems must be efficient in terms of energy, power, area, and cost. Moreover, many embedded systems are required to be flexible enough to be reused for different software versions. Multi-core systems working in SIMD/SPMD (Single Instruction Multiple Data/Single Program Multiple Data) fashion have been shown to be powerful executes for data-intensive computations [1, 2] and prove very fruitful in pixel processing domain [3, 4]. Their parallel architecture strongly reduces the amount of memory access and the clock speed, thereby enabling higher performance [5, 6]. Such multi-core systems are made up of an array of processing elements (PEs) that synchronously execute the same program on different local data. These parallel architectures are differentiated by their design, which is cost effective for different applications by increasing or reducing the number of Processors.

Today, the problem of designing suitable multiprocessor architecture tailored for a target application field raises the need for a fast and efficient multiprocessor system on chip (MPSoC) environment. The implementation of image processing applications on MPSoC system will need to exploit the parallelism and the pipelining in algorithms with the hope of delivering significant reduction in execution times. using the advantage of parallelization on homogeneous MPSoCs and to reducing the programming effort, the proposed design methodology offers simultaneously execution of multiple instructions from a different processor at same time.

Such multicore systems are made up of an array of processing elements (PEs) that synchronously execute the same program on different local data and can communicate through an interconnection network. This architecture NiosII economic processors will be used to reduce overhead on single processor for performing image processing application and an assign unique task to different processors to increase level of parallelism, achieving better performance and reducing power consumption.

II. LITERATURE SURVEYS

A.Kulmala et.al presented different multiprocessor architectures using NIOS II soft core processor to increase the efficiency in terms of GOPS per watt, architecture is based on SIMD/SPMD it is implemented on FPGA devices.

C. M. Witten brink et.al proposed architecture consist of 512 cores, example is Fermi processor. These architectures have some limitations for accessing memory because all cores share same memory also high power consumption therefore not suitable for embedded application.

H. M. Waidyasooriya et.al proposed architecture which is based on heterogeneous multicore system. it consist of 1-diamantational & 2-diamantional PE Array.A custom hardware address generation unit (AGU) is used, reprogramming is done to reduced no. of clock cycles. It required minimum no. of clock cycles compared to AGU based address generation.

S. Y. C. Li et.al proposed parallel SIMD processor based on FPGA. It consists of 95 Processor & Memory on chip. This architecture introduced to implements RC4 Key engines.

D. Kissler et.al, proposed an architectures which is based on coarse grain reconfigurable system. It provide dynamic reconfigurable network. The programming elements used in this design required limited instruction memory and executes only digital signal processing instruction.

T. Dorta et.al, proposed several on chip multicore platforms, which is used to increase efficiency of the system.

III. CONCLUSIONS

Design of Multisoft core processor architecture will be implementing on reconfigurable platform to achieve better performance in terms of fast processing and low power consumptions. This can be used according to requirements such as performance and cost, suitable for image processing, digital signal processing and video signal processing.
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applications. This paper provides objective of design of multisoft core processor architectures implementation on reconfigurable platform using nios II processor and most of the application areas where it is used. Literature survey provides various multi soft core processor architectures designs and gives detail information about it.

REFERENCES


