Switching Loss Reduction in a Cascaded Multilevel Inverter with Reduced Number of Components

P. Kalayarasan[1] K. Nandakumar[2]
[1]P.G Scholar [2]Assistant Professor
[1,2]Department of Electrical & Electronics Engineering
[1,2]E.G.S.Pillay Engineering College, Nagapattinam

Abstract— A new general cascaded multilevel inverter with single carrier level shift PWM is proposed in this paper. The proposed topology requires a lesser number of dc voltage sources and power switches and consists of lower blocking voltage on switches, which results in decreased complexity and total cost of the inverter. These abilities obtained within comparing the proposed topology with the conventional topologies. Moreover, a new algorithm to determine the magnitude of dc voltage sources is proposed. In which only one carrier signal is used and compared with reference signal. Depends upon the level or RMS value of output voltage, the level of carrier signal is determined. Based on the level determined, the carrier signal is shifted and compared with reference signal. The proposed technique completely eliminates the switching transition in the lower levels. So it reduces switching loss and also improves the power quality. The performance and functional accuracy of the proposed topology using the new algorithm in generating all voltage levels for a 31-level inverter are confirmed by MATLAB simulation and experimental results.

Key words: Cascaded multilevel inverter, developed H-bridge, multilevel inverter, voltage source inverter

I. INTRODUCTION

NOWADAYS, multilevel inverters have received more attention for their ability on high-power and medium voltage operation and because of other advantages such as high power quality, lower order harmonics, lower switching losses, and better electromagnetic interference [1], [2]. These inverters generate a stepped voltage waveform by using a number of dc voltage sources as the input and an appropriate arrangement of the power-semiconductor-based devices [3].Three main structures of the multilevel inverters have been presented: “diode clamped multilevel inverter,” “flying capacitor multilevel inverter,” and “cascaded multilevel inverter” [4].The cascaded multilevel inverter is composed of a number of single-phase H-bridge inverters and is classified into symmetric and asymmetric groups based on the magnitude of dc voltage sources. In the symmetric types, the magnitudes of the dc voltage sources of all H-bridges are equal while in the asymmetric types, the values of the dc voltage sources of all H-bridges are different. In recent years, several topologies with various control techniques have been presented for cascaded multilevel inverters [5]–[8]. In [4] and [9]–[12], different symmetric cascaded multilevel inverters have been presented. The main advantage of all these structures is the low variety of dc voltage sources, which is one of the most important features in determining the cost of the inverter. On the other hand, because some of them use a high number of bidirectional power switches, a high number of metal oxide semiconducting field effect transistors (MOSFETs) are required, which is the main disadvantage of these topologies.

An asymmetric topology has been presented in [12]. The main Disadvantage of this structure is related to its bidirectional power switches, which cause an increase in the number of MOSFETs and the total cost of the inverter. In [11], a new topology with news algorithms have been presented, which reduce the number of required power switches but increase the variety of dc voltage sources. In [1], [4] and [8], several algorithms for determining the magnitudes of dc voltage sources for the conventional cascaded multilevel inverter have been presented. The major advantage of this topology and its algorithms is related to its ability to generate a considerable number of output voltage levels by using a low number of dc voltage sources and power switches but the high variety in the magnitude of dc voltage sources is their most remarkable disadvantage. In this paper, in order to increase the number of output voltages levels and reduce the number of power switches, driver circuits, and the total cost of the inverter, a new topology of cascaded multilevel inverters is proposed. It is important to note that in the proposed topology, the unidirectional power switches are used. Then, to determine the magnitude of the dc voltage sources, a new algorithm is proposed. Moreover, the proposed topology is compared with other topologies from different points of view such as the number of MOSFETs, number of dc voltage sources, the variety of the values of the dc voltage sources, and the value of the blocking voltages per switch. Finally, the performance of the proposed topology in generating all voltage levels through a 31-level inverter is confirmed by simulation using MATLAB software and experimental results.

Multilevel inverters have been attracting wide industrial interest. They are considered an attractive alternative in order to reduce switch stress. The main characteristic of these converters is an output waveform with multiple voltage levels. In recent decades, an extensive array of multilevel structures has appeared for instance, the cascaded H-bridge, neutral point clamped, and flying capacitor. The Cascaded H-bridge multilevel inverter is a popular topology and has found widespread applications in industry, for instance, in high power medium-voltage drives and reactive power compensation. Most multilevel inverters have an arrangement of switches and capacitor voltage sources.

By a proper control of the switching devices, these can generate stepped output voltages with low harmonic distortions. These multilevel inverters are widely used in manufacturing factories and acquired public recognition as one of the new power converter fields because they can overcome the disadvantages of traditional pulse width-modulation (PWM) inverters.

A cascaded H-bridge multilevel inverter which employs one single dc input power source and isolated three-phase low-frequency transformers. By the proposed circuit configuration, a number of transformers can be reduced, compared with traditional three-phase multilevel inverters using single-phase transformers. Therefore, an economical and efficient inverter can be designed. Basically, the switching frequency of each H-bridge inverter is uniform with output fundamental frequency. The delay angles of each switch are calculated by the Sinusoidal PWM method on the basis of the area of each switch. All delay angles can be determined by applying the linearization method to each area. This approach is useful to eliminate low harmonic components of the output voltage.

A. *Types of Multi Level Inverter:*

The general structure of multi-level converter is to synthesize a near sinusoidal voltage from several levels of dc voltages, typically from capacitor voltage sources. As number of levels increases, the synthesized output waveform has more steps, which provides a staircase wave that approaches a desired waveform. Also, as steps are added to waveform, the harmonic distortion of the output wave decreases, approaching zero as the number of voltage levels increases. The Multi-level inverters can be classified into three types.

- Diode – clamped Multi-level inverter
- Flying – capacitor Multi-level inverter
- Cascade Multi-level inverter

B. *Diode- Clamped Multilevel Inverter:*

A diode – clamped (m-level) inverter (DCMLI) typically consists of (m-1) capacitor on the dc bus and produces m levels on the phase voltages. Figure shows full bridge five level diode clamped converter. The numbering order of the switches is Sa1, Sa2, Sa3, Sa4,S'a1, S'a2, S'a3, S'a4. The dc bus voltage consists of four capacitors C1, C2, C3, and C4. For a dc voltage Vdc, the voltage across each capacitor is V dc/4, and each devices voltage stress is limited to one capacitor voltage level V dc/4 through clamping diodes. An m-level inverter leg requires (m-1) capacitors, 2(m-1) switching devices and (m-1) X (m-1) clamping diodes.

To produce a stair case output, let us consider only one leg of five levels Inverter, as shown in Figure 1. A single phase ridge with one leg is shown in figure 1.The steps to synthesize the five level voltages are as follows

a) Voltage level Van= V dc; turn on all upper switches S1, S2, S3 and S4.

b) Voltage level Van= V dc/2, turn on the switches S2, S3, S4 and S1′.

c) Voltage level Van= 0, turn on the switches S3, S4, S1′ and S2′.

d) Voltage level Van= - V dc/2 turn on the switches S4, S1′, S2′, S3′.

e) Voltage level Van= - V dc; turn on all lower switches S1′, S2′, S3′ and S4′.

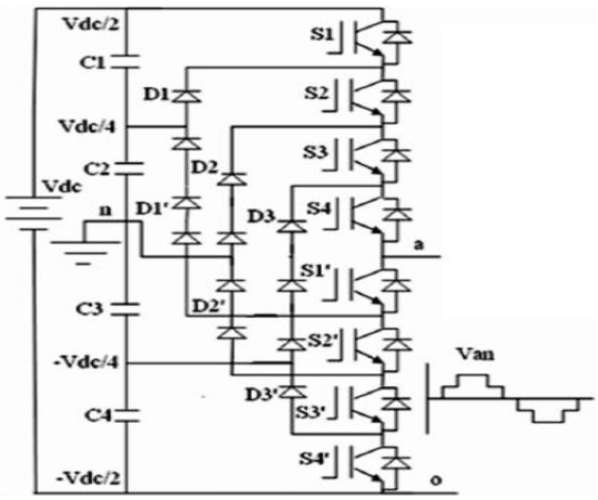

Fig. 1: Single phase Diode clamped inverter

C. *Flying Capacitor Multilevel Inverter:*

The figure .2 shows a single phase full bridge 5-level inverter based on flying capacitors. Each phase like has an identical structure. Assuming that each capacitor has the same voltage rating, the series connection of the capacitors indicates the voltage level between calming points. All phase legs share the DC link capacitors C1 to C4.

1) *Principle of Operation:*

To produce a staircase output voltage, the switching instants of MOSFETS will be shown below.

- Voltage level Van = Vdc/2, turn on all upper switches S1 -S4.
- Voltage level Van = Vdc/4, there are three combinations.
  - Turn on switches S1, S2, S3 and S1′. (Van = Vdc/2 of upper C4s - Vdc/4 of C1s).
  - Turn on switches S2, S3, S4 and S4′. (Van = 3Vdc/4 of upper C3s - Vdc/2 of C4s).
  - Turn on switches S1, S3, S4 and S3′. (Van= Vdc/2 of upper C4s – 3Vdc/4 or C3s + Vdc/2 of upper C2,,).
- Voltage level Van= 0, turn on upper switches S3, S4, and lower switch S1′, S2′.
- Voltage level Van= -Vdc/4, turn on upper switch S1 and lower switches S1′, S2′ and S3′.
- Voltage level Van= -Vdc/2, turn on all lower switches S1′, S2′, S3′ and S4′.

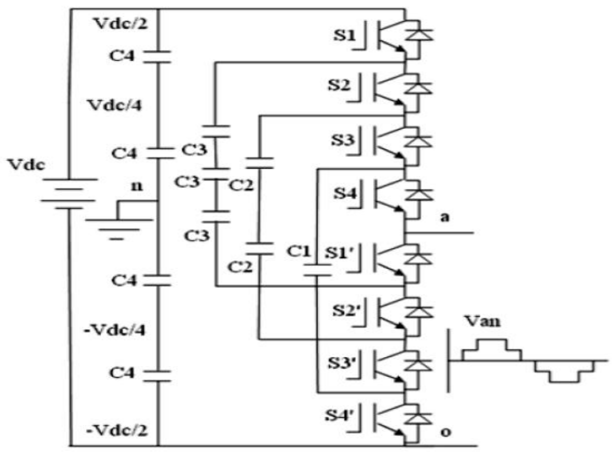

Fig. 2: single phase flying capacitor inverter

D. Cascaded Multi-Level Inverter:

A relatively new converter structure called Cascaded Multi-level inverter, can avoid extra clamping diodes or voltage balancing capacitors. The converter topology used here is based on the series connection of single phase inverters with separate DC sources.

II. PROPOSED MULTILEVEL INVERTER CONFIGURATIONS

The different topologies by with H-bridge are designed are:

- Cascade H-bridge
- Hybrid H-bridge

A. Cascade H-Bridge:

Figure.3 shows the basic block of cascade H-bridge Multi-level inverter and its associated switching instants. As shown its consists of four power devices and a DC source. The switching states for four power devices are constant i.e., When S1 is on, S2 cannot be on and vice versa. Similarly with S3 and S4

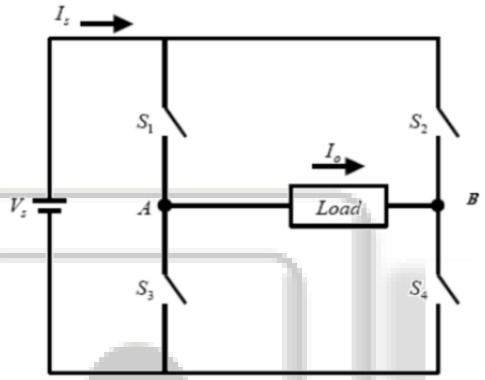

Fig. 3: Block of a h-bridge Multi-level inverter

Figure.3 shows the power circuit for one phase of multi-level inverter. The resulting voltage ranges from +3Vdc to -3Vdc and the staircase are nearly sinusoidal, even without filtering.

B. Hybrid H-Bridge:

A hybrid H-bridge inverter consists of a series of H-bridge inverter units. The general function of this Multi-level inverter is to synthesize a desired voltage form several DC sources (SDCSs). Each SDCS is connected to an H-bridge inverter. The AC terminal voltages of different level inverters are connected in series. Unlike diode clamp or flying capacitors inverters the hybrid H-bridge inverter does not require any voltage clamping diodes or voltage-balancing capacitors.

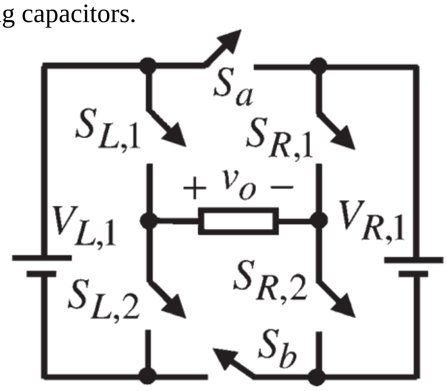

Fig. 4: Block of hybrid H-bridge Multi-level inverter

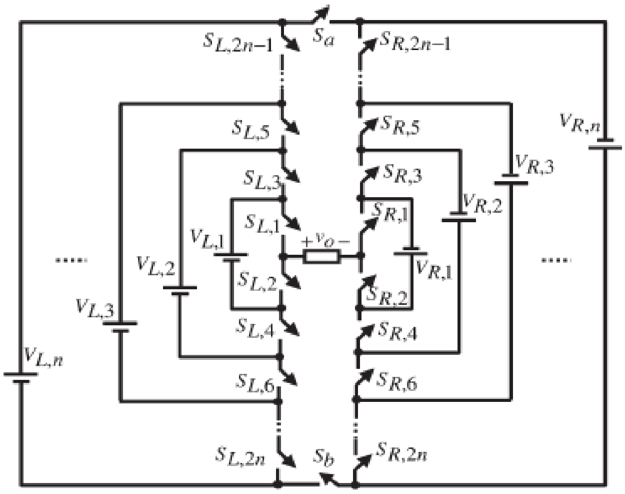

Fig. 5: General structure of H-bridge Multi-level inverter

The magnitudes of the dc voltage sources of the proposed 31-level inverter are recommended as follows:

$$V_{L,1} = V_{dc}$$
$$V_{R,1} = 2V_{dc}$$
$$V_{L,2} = 5V_{dc}$$
$$V_{R,2} = 10V_{dc}.$$

The proposed inverter can generate all negative and positive voltage levels from 0 to 15*V*dc with steps of *V*dc

The proposed inverters are comprised of six unidirectional power switches (Sa, Sb, SL,1, SL,2, SR,1, and SR,2) and two dc voltage sources (VL,1 and VR,1). In this paper, these topologies are called developed H-bridge. As shown in Fig. 1, the simultaneous turn-on of SL,1 and SL,2 (or SR,1 and SR,2) causes the voltage sources to short-circuit. Therefore, the simultaneous turn-on of the mentioned switches must be avoided.

In addition, Sa and Sb should not turn on, simultaneously. The difference in the topologies illustrated in Fig. 1 is in the connection of the dc voltage sources polarity. Table I shows the output voltages of the proposed inverters for different states of the switches. In this table, 1 and 0 indicate the ON- and OFF-states of the switches, respectively. As it is obvious from Table I, if the values of the dc voltage sources are equal, the number of voltage levels decreases to three. Therefore, the values of dc voltage sources should be different to generate more voltage levels without increasing the number of switches and dc voltage sources. In the magnitudes of VL,1 and VR,1 should be considered 3pu and 1pu, respectively. Similarly, for the topology. The magnitudes of VL,1 and VR,1 should be considered 2pu and 1pu, respectively. Considering the aforementioned explanations, the total cost of the proposed topology is low because dc voltage sources with low magnitudes are needed. By developing the seven-level inverter the 31-level inverter shown in Fig. 2 can be proposed.

This topology consists of ten unidirectional power switches and four dc voltage sources. According to Fig. 2, if the power switches of (SL,1, SL,2), (SL,3, SL,4), (SR,1, SR,2), and (SR,3, SR,4) turn on simultaneously, the dc voltage sources of VL,1, VL,2, VR,1, and VR,2 will be short-circuited, respectively. Therefore, the simultaneous turn-on of these switches should be avoided.

In addition, Sa and Sb should not turn on simultaneously. It is important to note that the 31-level topology can be provided through where the only difference will be in the polarity of the applied dc voltage sources. By developing the proposed 31-level inverter. This topology consists of 14 unidirectional power switches and 6 dc voltage sources. Similarly, by developing the proposed basic topology, a general topology, as shown in Fig. 4, can be proposed. The general topology consists of 2n dc voltage sources (n is the number of the dc voltage sources on each leg) and 4n + 2 unidirectional power switches.

III. EXISTING SYSTEM SIMULATION

A. *Existing System:*

The MATLAB diagram of the existing system is shown in Fig. 4s

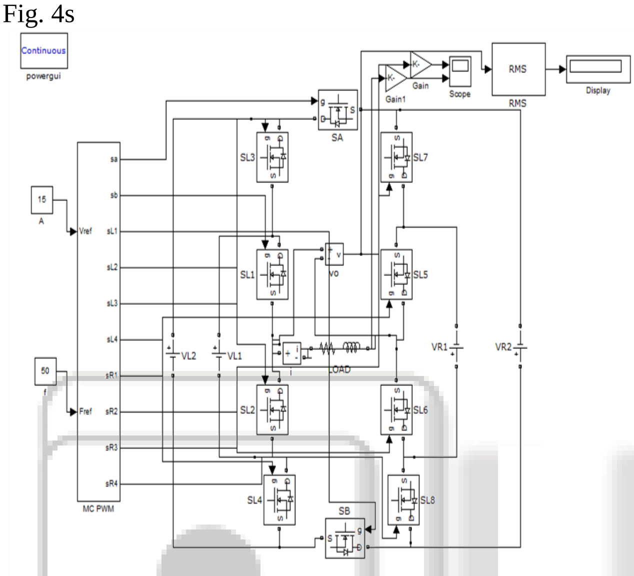

Fig. 5: Existing System.

The above circuit shows the Simulation of 31 level H-bridge inverter

B. *Simulink Model of MCPWM:*

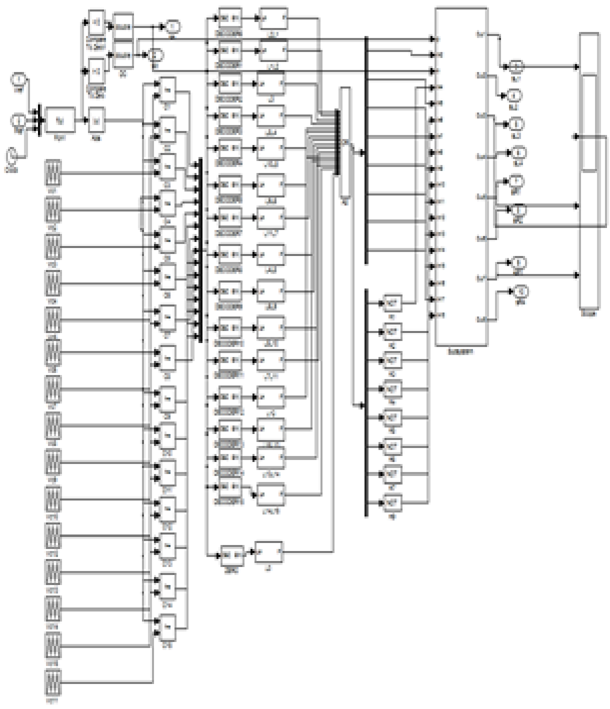

Fig. 6: Existing System MCPWM.

C. *Switching Pulses (Sl1, Sl3, SR1, SR3):*

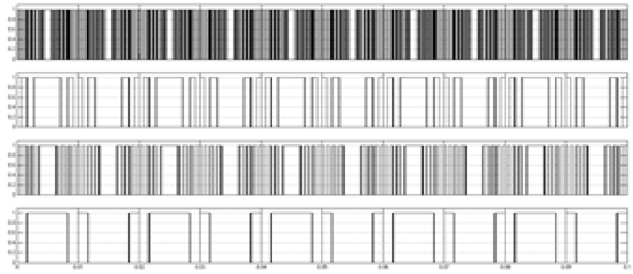

Fig. 7: Existing System switching pulses.

The switching pulses for the switches are applied based on the time duration calculated. Based on the time duration value, the switching pattern will be assigned and pulses are applied.

D. *Output Waveforms:*

The voltage, current waveforms are shown in Fig. 7

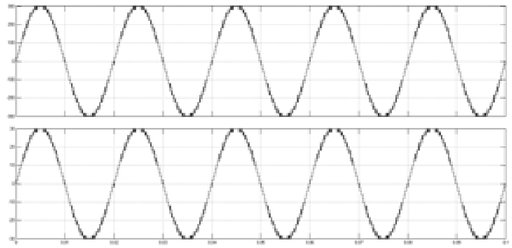

Fig. 8: Output voltage and current waveform.

Fig.8 shows the wave form of output voltage Vs time and output current Vs time. Voltage and current is taken in the y-axis and time in the x-axis. Here 230V is given as output voltage and 23A is output current.

E. *FFT Analysis:*

The below fig shows the FFT analysis of Existing system. Magnitude is taken in the y-axis and Frequency in the x-axis. Here Fundamental frequency (50Hz) =304.4 THD=3.47%

The FFT analysis result of the output ac phase voltage is shown in Fig. 9. It shows that the harmonics is little compared to the base-frequency component.

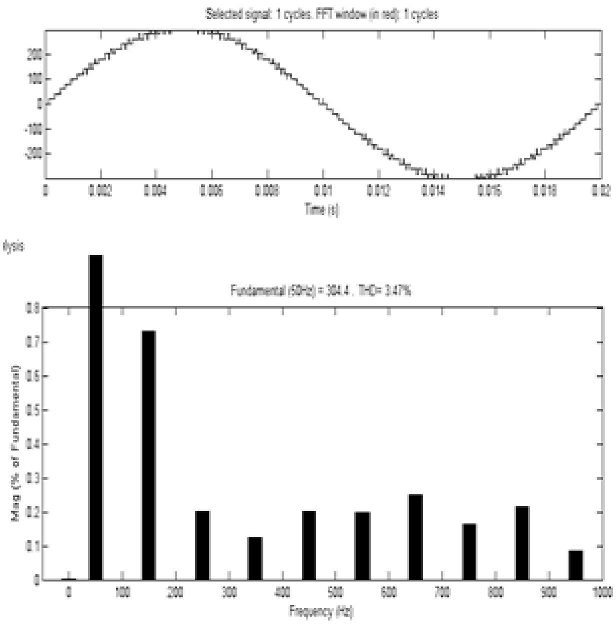

Fig. 9: FFT Analysis of Existing System

IV. PROPOSED SYSTEM SIMULATION

A. Proposed System:

The MATLAB diagram of the proposed system is shown in Fig. 10.

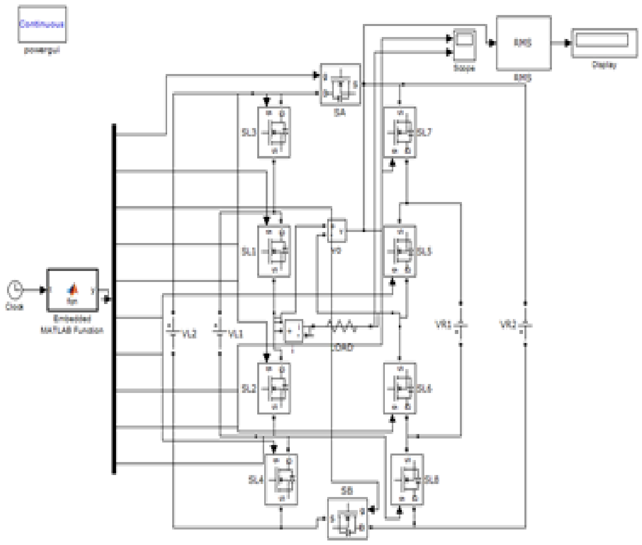

Fig. 10: Proposed system simulation

The above circuit shows the Simulation of single phase hybrid cascaded multi-level inverter. Each leg contains ten switches totally ten switches needed for three phase. Here MOSFETs act as a switch due to high power application. Pulse for MOSFETs switch obtains from SCLSPWM technique. The outputs of the inverter are multilevel voltages with less harmonics and lower dv/dt, eliminates the switching transition in the lower levels. So it reduces switching loss and also which is helpful to improve the power quality.

B. Output Waveforms:

The output voltage, current waveforms are shown in Fig. 11

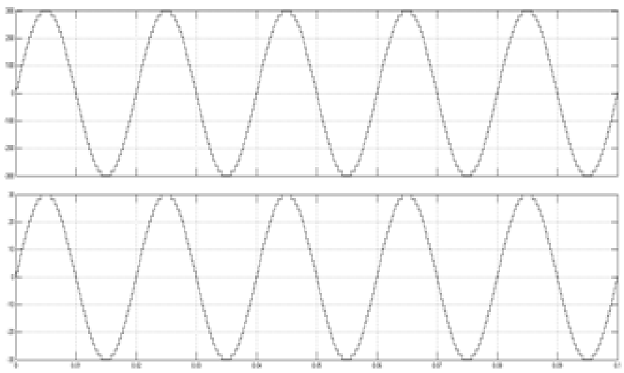

Fig. 11 Output voltages and current waveform.

Fig.11 shows the wave form of output voltage Vs time and output current Vs time. Voltage and current is taken in the y-axis and time in the x-axis. Here 230V is given as output voltage and 23A is output current.

The ac output voltage and output current are shown in Figs. 11 As the lag between the voltage and current phase, when the phase voltage change direction, the H-bridge will change its switching state too. But the phase ac current will change its direction after a period of time, so the direction of the dc bus current is reversed when the directions of phase voltage and current are different. The reversed dc bus current also reflects the reactive power of the load.

The output of the circuit is multilevel ac voltages where the number of levels is proportional to the power quality. So the output ac voltage is nearly the ideal sinusoidal wave which can improve the control performance of the lower switching losses and also improve the power quality.

C. FFT Analysis:

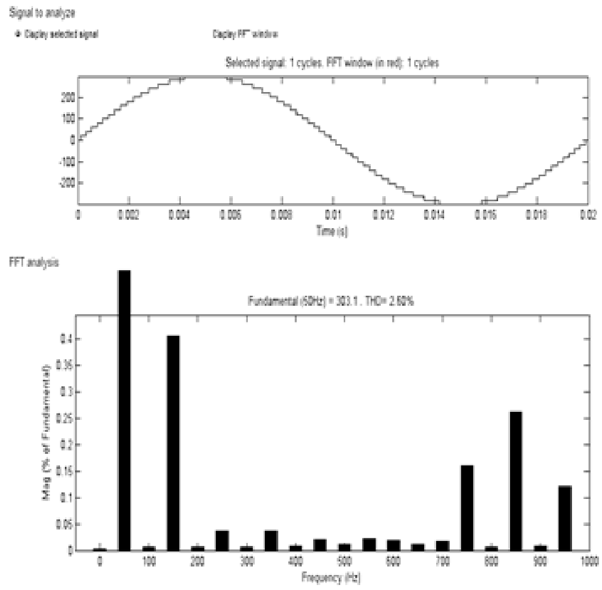

Fig. 12: FFT Analysis of Proposed system

Fig.12 shows the FFT analysis of Existing system. Magnitude is taken in the y-axis and Frequency in the x-axis. Here Fundamental frequency (50Hz)=303 THD=2.60%

The FFT analysis result of the output ac phase voltage is shown in Fig. 13. It shows that the harmonics is little compared to the base-frequency component.

V. PULSE GENERATION PROGRAM

A. M File for Pulse Generation:

1) Algorithm:

Step 1: Initialize the local variables

Step 2: Check for the time value

Step 3: If the time value satisfies the desired value, generate the corresponding switching pattern

Step 4: If the condition is not satisfied then checks for other conditions. If it satisfies the follow step 3 otherwise repeat the step 4

Step 5: End of the program.

Simplicity and to the good results it guarantees in all the operating conditions, including “over modulation,” which allows first harmonic. A complete analysis of both bipolar (for two-level inverters) and unipolar (for three-level inverters) methods has been widely. We now develop a analysis of the MCPWM method for multilevel inverters. We refer to the system outlined in Fig.4.3.1.For the proposed multilevel generalization of the PWM method; we take as a starting point the unipolar technique. The idea we follow is to use several triangular carrier signals, keeping only one modulating sinusoidal signal. If an N-level inverter is employed, N - 1 carrier will be needed.

B. Simulation of Pulse Generation Program:

```
function y = fcn(t)
%#eml
f=50;
r=sin(2*pi*f*t);
ar=abs(r);
 if ar<= 0.5/15
 p1=0;p2=1;p3=0;p4=1;p5=0;p6=1;p7=0;p8=1;
 elseif ar<1.5/15
 p1=1;p2=0;p3=0;p4=1;p5=0;p6=1;p7=0;p8=1;
 elseif ar<2.5/15
 p1=0;p2=1;p3=0;p4=1;p5=1;p6=0;p7=0;p8=1;
 elseif ar<3.5/15
 p1=1;p2=0;p3=0;p4=1;p5=1;p6=0;p7=0;p8=1;
 elseif ar<4.5/15
 p1=0;p2=1;p3=1;p4=0;p5=0;p6=1;p7=0;p8=1;
 elseif ar<5.5/15
 p1=1;p2=0;p3=1;p4=0;p5=0;p6=1;p7=0;p8=1;
 elseif ar<6.5/15
 p1=0;p2=1;p3=1;p4=0;p5=1;p6=0;p7=0;p8=1;
 elseif ar<7.5/15
 p1=1;p2=0;p3=1;p4=0;p5=1;p6=0;p7=0;p8=1;
 elseif ar<8.5/15
 p1=0;p2=1;p3=0;p4=1;p5=0;p6=1;p7=1;p8=0;
 elseif ar<9.5/15
 p1=1;p2=0;p3=0;p4=1;p5=0;p6=1;p7=1;p8=0;
 elseif ar<10.5/15
 p1=0;p2=1;p3=0;p4=1;p5=1;p6=0;p7=1;p8=0;
 elseif ar<11.5/15
 p1=1;p2=0;p3=0;p4=1;p5=1;p6=0;p7=1;p8=0;
 elseif ar<12.5/15
 p1=0;p2=1;p3=1;p4=0;p5=0;p6=1;p7=1;p8=0;
 elseif ar<13.5/15
 p1=1;p2=0;p3=1;p4=0;p5=0;p6=1;p7=1;p8=0;
 elseif ar<14.5/15
 p1=0;p2=1;p3=1;p4=0;p5=1;p6=0;p7=1;p8=0;
 else
 p1=1;p2=0;p3=1;p4=0;p5=1;p6=0;p7=1;p8=0;
 end
 if r>0
       p9=0;p10=1;
  y=[p9 p10 p1 p2 p3 p4 p5 p6 p7 p8];
 else
        p9=1;p10=0;
  y=[p9 p10 p2 p1 p4 p3 p6 p5 p8 p7];
 end
```

Fig. 12: Output waveform for pulse generation circuit

SL.NO	**SL1**	**SL2**	**SL3**	**SL4**	**SR1**	**SR2**	**SR3**	**SR4**	**Sa**	**Sb**	**V0**
1	1	0	0	1	0	1	0	1	0	**1**	VL1
2	0	1	0	1	1	0	0	1	0	**1**	VR1
3	1	0	0	1	1	0	0	1	0	**1**	VL1+VR1
4	0	1	1	0	0	1	0	1	0	**1**	VL2-VL1
5	1	0	1	0	0	1	0	1	0	**1**	VL2
6	0	1	1	0	1	0	0	1	0	**1**	VL2+VL1
7	1	0	1	0	1	0	0	1	0	**1**	VL2+VR1
8	0	1	0	1	0	1	1	0	0	**1**	VR2-VR1
9	1	0	0	1	0	1	1	0	0	**1**	VR2-VL1
10	0	1	0	1	1	0	1	0	0	**1**	VR2
11	1	0	0	1	1	0	1	0	0	**1**	VL1+VR2
12	0	1	1	0	0	1	1	0	0	**1**	VR1+VR2
13	1	0	1	0	0	1	1	0	0	**1**	VL1+VR1+VR2
14	0	1	1	0	1	0	1	0	0	**1**	VR2+VL2-VL1
15	1	0	1	0	1	0	1	0	0	**1**	VL2+VR2
16	0	1	0	1	0	1	0	1	0	**1**	0
16	0	1	0	1	0	1	0	1	1	**0**	0
17	1	0	0	1	0	1	0	1	1	**0**	-VL1
18	0	1	0	1	1	0	0	1	1	**0**	-VR1
19	1	0	0	1	1	0	0	1	1	**0**	-(VL1+VR1)
20	0	1	1	0	0	1	0	1	1	**0**	-(VL2-VL1)
21	1	0	1	0	0	1	0	1	1	**0**	-VL2
22	0	1	1	0	1	0	0	1	1	**0**	-(VL2+VL1)
23	1	0	1	0	1	0	0	1	1	**0**	-(VL2+VR1)
24	0	1	0	1	0	1	1	0	1	**0**	-(VR2-VR1)
25	1	0	0	1	0	1	1	0	1	**0**	-(VR2-VL1)
26	0	1	0	1	1	0	1	0	1	**0**	-VR2
27	1	0	0	1	1	0	1	0	1	**0**	-(VL1+VR2)
28	0	1	1	0	0	1	1	0	1	**0**	-(VR1+VR2)
29	1	0	1	0	0	1	1	0	1	**0**	-(VL1+VR1+VR2)
30	0	1	1	0	1	0	1	0	1	**0**	-(VR2+VL2-VL1)
31	1	0	1	0	1	0	1	0	1	**0**	-(VL2+VR2)

Table 1: Output Voltages for the 31 Level Inverter

VI. CONCLUSION

In this paper, multilevel inverters to generate 31 voltage levels at the output are proposed. The new algorithm to determine the magnitude of the dc voltage sources has been proposed. The proposed single carrier level shift PWM is compared with the existing multi carrier PWM. According to the comparison results, the proposed topology requires a lesser number of MOSFETs, power diodes, driver circuits, and dc voltage sources. Moreover, the magnitude of the blocking voltage of the switches is lower than that of conventional topologies. The existing Multi carrier PWM technique produces the THD of 3.47% at maximum voltage of 304V. The proposed single carrier level shift PWM technique produces the THD of 2.6% at maximum voltage of 303V. It shows the improvement in the harmonic profile. However, the proposed topology has a higher number of variety of dc voltage sources in comparison with the others. The performance accuracy of the proposed topology was verified through the MATLAB simulation.

REFERENCES

[1] A New General Topology for Cascaded Multilevel Inverters With Reduced Number of Components Based on Developed H-Bridge Ebrahim Babaei, Member, IEEE, Somayeh Alilu, and Sara Laali, Student Member, IEEE
[2] E. Babaei and S. H. Hosseini, “Charge balance control methods for asymmetrical cascade multilevel converters,” in Proc. ICEMS, Seoul, Korea, 2007, pp. 74–79.
[3] K. Wang, Y. Li, Z. Zheng, and L. Xu, “Voltage balancing and fluctuation suppression methods of floating capacitors in a new modular multilevel converter,” IEEE Trans. Ind. Electron., vol. 60, no. 5, pp. 1943–1954, May 2013.
[4] J. Ebrahimi, E. Babaei, and G. B. Gharehpetian, “A new topology of cascaded multilevel converters with reduced number of components for high-voltage applications,” IEEE Trans. Power Electron., vol. 26, no. 11, pp. 3109–3118, Nov. 2011.
[5] Multilevel Inverters: A Survey of Topologies, Controls, and Applications José Rodríguez, Senior Member, IEEE, Jih-Sheng Lai, Senior Member, IEEE, and Fang Zheng Peng, Senior Member, IEEE Operation and Design of Multilevel Inverters- Dr. Keith Corzine University of Missouri – Rolla
[6] N. Abd Rahim, M. F. Mohamad Elias, andW. P. Hew, “Transistor-clamped H-bridge based cascaded multilevel inverter with new method of capacitor voltage balancing,” IEEE Trans. Ind. Electron., vol. 60, no. 8, pp. 2943– 2956, Aug. 2013.
[7] M. Farhadi Kangarlu and E. Babaei, “A generalized cascaded multilevel inverter using series connection of submultilevel inverters,” IEEE Trans.Power Electron., vol. 28, no. 2, pp. 625–636, Feb. 2013.
[8] S. R. Pulikanti, G. Konstantinou, and V. G. Agelidis, “Hybrid seven-level cascaded active neutral-point-clamped-based multilevel converter under SHE-PWM,” IEEE Trans. Ind. Electron., vol. 60, no. 11, pp. 4794–4804, Nov. 2013.
[9] Y. Hinago and H. Koizumi, “A single-phase multilevel inverter using switched series/parallel dc voltage sources,” IEEE Trans. Ind. Electron., vol. 57, no. 8, pp. 2643–2650, Aug. 2010.
[10] G. Waltrich and I. Barbi, “Three-phase cascaded multilevel inverter using ower cells with two inverter legs in series,” IEEE Trans. Ind. Appl., vol. 57, no. 8, pp. 2605–2612, Aug. 2010.
[11] W. K. Choi and F. S. Kang, “H-bridge based multilevel inverter using PWM switching function,” in Proc. INTELEC, 2009, pp. 1–5.
[12] E. Babaei, M. Farhadi Kangarlu, and F. Najaty Mazgar, “Symmetric and asymmetric multilevel inverter topologies with reduced switching devices,” Elect. Power Syst. Res., vol. 86, pp. 122–130, May 2012.

