Design of a High Frequency Low Voltage CMOS Operational Amplifier

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Abstract— This paper presented a method for the design of a high frequency CMOS operational amplifier. The OPAMP is designed using tsmc 0.18 micron CMOS technology which operates at 2.5V power supply. This is a two stage CMOS OPAMP which employs a miller capacitor. To design a two stage OPAMP is a multi-dimensional optimization problem where optimization of one or more parameters may easily result into degradation of others. The OPAMP is designed to exhibits a unity gain frequency of 2.2 GHz exhibits a gain of 54.11db with 60˚ phase margin. Design has been carried out in Pspice tool.

Key words: CMOS analog circuit, Operational amplifier, Miller compensation, High gain bandwidth, Low voltage

I. INTRODUCTION

The electronics industry has exploded over the few years. The MOS market is dominating the largest segment of total worldwide sales. The total combined MOS revenue approx 75% of total worldwide sales which composed primarily of memory, micro and logic sales showing the strength of CMOS technology. CMOS technology has an edge over NMOS technology due to relatively simple circuit configuration and flexibility of design. In analog processing system operational amplifiers are key elements. In an analog circuit OPAMP can be said to be the main bottleneck. Ideally they have an infinite voltage gain and perform the function of a voltage controlled current source. Operational amplifiers are an integral part of many analog and mixed signal systems. Functions ranging from dc bias generation to high speed amplification or filtering can be implementing using OPAMP with vastly different levels of complexity. As the supply voltage and the transistor channel length scale down with each generation of COMS technologies, the design of operational amplifier continues to pose a challenge. Power dissipation can be reduced by reducing either power supply or total current in the circuit or by reducing the both. As the input current is lowered though power dissipation is reduced, dynamic range is degraded. As the supply voltage decreases, it also becomes increasingly difficult to keep transistors in saturation with the voltage headroom available. Another concern that draws from the supply voltage scaling is the threshold voltage of the transistor. A decrease in supply voltage without a similar decrease in threshold voltage leads to biasing issues. In order to achieve the required degree of stability, generally indicated by phase margin, other performance parameters are usually compromised.

With the relentless trend toward reduced power supply voltages, designing of high performance analog integrated circuit is becoming increasingly exigent. There is a tradeoff among speed, power, gain, and other performance parameters at the large supply voltages. For the operational amplifier architecture these parameter present contradictory choice. The two most important properties of analog circuits are speed and accuracy, however optimizing circuits for both aspect leads to contradictory demands. Design of a operational amplifier which has high gain with high gain bandwidth has been a difficult problem. To evade this problem there have been several circuit approaches. The method handles wide variety of specifications and constraints. In this, we formulate the CMOS operational amplifier design problem and their aspect ratios. The variation in the performance of the operational amplifier with variations in the width and length of the MOS and the effect of the gate oxide thickness scaling is discussed. The simulation result has been obtained by tsmc 0.18 micron CMOS technology.

II. RELATED WORK

The operational amplifier is a really significant and widely used building block in the analog and mixed signal circuit design field. The performance of Op-amp in the integrated circuit is affects overall performance of the system. Due to its popularity a lot of work on it has been done. A simple design process for two stage CMOS operational amplifier for integrated into an analog design based CAD tool have defined by G. Palmisano et al [3], in 2001. They discussed about typical frequency compensation techniques for high gain bandwidth product. A two stage RC miller compensated operational amplifier has been designed by D.S shylu et al [17], which is suitable for ADC application with comparatively low phase margin. Vikas agarwal et al [14] used the bulk-driven technology which yields the low power consumption and large input CMR but exhibits a very low gain bandwidth. The approach used by R.K Baruah [21], giving low power consumption and operational amplifier is operated at low voltage but it presented a very low unity gain frequency. A simple two stage CMOS operational amplifier has been designed by Purvi .D Patel [21] which result in lower power consumption and operates on low voltage as well. Vikas Sharma et al [19], used cascade technique to increase the dc gain. The approach adopted gives a high unity gain bandwidth, high gain with low power dissipation. The approach used by P.K .Sinha et al [16] improves the slew rate of the operational amplifier which operates on low voltage. M. Alioto [18] presented a paper about the DC behavior of subthreshold CMOS logic for ultra-power circuit design perspective. They provides an effective implementation of small signal as well as large signal model for subthreshold region operation of MOS transistor. The multi-stage design [23] improves the settling time and gain but leads to the decrease of the phase margin and unity gain frequency. The research work [22] insists the incorporation of pseudo-cascode compensation instead of Miller compensation to increase the unity gain frequency up to 450MHz. But it is seen that this approach degrades the phase margin with the increase of unity gain frequency. Mahattanakaul and Chutichatuporn [20] have improver the design procedure that allows the C_c a wider range, which provides a higher degree of freedom in the trade-off between noise and power consumption. Design procedures reported in literatures have not given much attention to the improvement of the unity gain frequency of operational amplifiers. Moreover, in these procedures, the effect of

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capacitive load on unity gain frequency, speed and power is not considered. In this work, an op amp has been designed which exhibits high unity gain frequency for optimized balancing of phase margin, gain, speed and power. A method is proposed to set a higher unity gain frequency of the OPAMP working with lower supply voltage. This allows the value of each circuit element of the amplifier (i.e. transistor aspect ratios, bias current and compensation capacitor) to be univocally related to the required electrical parameters.

III. OP AMP STRUCTURE

Several new topologies have evolved and have been employed in various applications, in past few years. Here we have chosen a simple differential pair amplifier(high noise immune) for input amplifier, common source amplifier (high gain) for output amplifier, a current mirror circuit (free from voltage sources; utilizing single current reference source) as a biasing circuit, and Miller compensation with nulling resistor in conjunction with a Miller capacitance in series with one other.

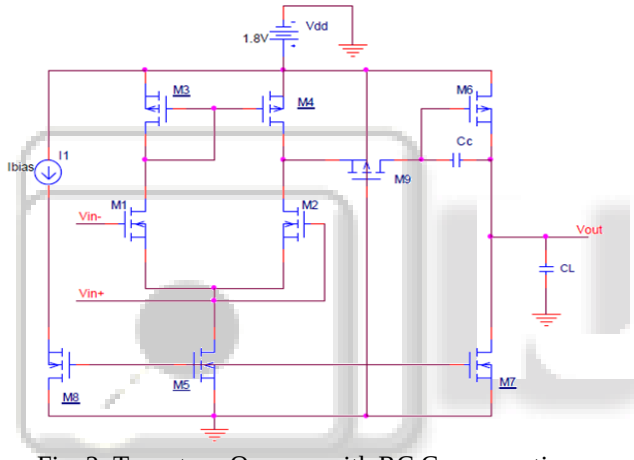

Fig. 2: Two stage Op-amp with RC Compensation

The topology is that of a standard CMOS Op-amp of the circuit designed. It consists of three subsections of the circuits, which are differential gain stage, second gain stage and bias strings.

IV. DESIGN APPROACH

A two stage CMOS Op amp is shown in figure 2. The first stage of this Op amp is consist of M1-M5 and M8 transistors, the second stage is consist of M6-M7 transistors and miller compensation capacitor C_C is used between the output and input of the second stage. All transistors used in this Op amp are operates in saturation region. The first stage is the differential stage, the differential signal is applied to the gate terminal of the transistor M1 and M2 respectively. These transistor M1 and M2 are two NMOS driver transistors used to convert the differential voltage to differential currents are given to the current mirrored load transistor M3 and M4. The transistor M5 and M8 are used to provide the biasing current to the differential stage. The output of differential stage is a single ended output signal and it gives the difference of the input signal with a constant gain. The second stage is a common source gain stage, the output of the first stage is applied to the gate of the M6, the transistor M7 is provides the bias current to the second stage and the output is taken from the drain terminal of the M6.
The DC gain of the first stage is

$$A_1 = -\frac{g_{m2}}{g_{ds2} + g_{ds4}}$$

The DC gain of the second stage is

$$A_2 = -\frac{g_{m6}}{g_{ds6} + g_{ds7}}$$

Overall gain of the Op-amp is

$$A_V = A_1 . A_2$$

$$A_V = \frac{g_{m1} g_{m6}}{(g_{ds2} + g_{ds4})(g_{ds6} + g_{ds7})}$$

Slew Rate of the Op-amp is

$$SR = \frac{I_5}{C_C}$$

Where I_5 is the current through the M5 transistor and it is the bias current of the input stage.
The Gain bandwidth of the Op-amp is

$$GB = \frac{g_{m1}}{C_c}$$

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V. SIMULATION RESULTS

The two stages OPAMP was designed using the model parameter of tsmc 0.18 micron CMOS process. The design parameters along with the electrical parameters yielded are as given in the table 1. This circuit operates efficiently in a closed loop feedback system, while high bandwidth makes it suitable for high speed applications. The circuit operates with a power supply of 2.5V and a load of 10fF. The dc gain found to be 54.11db and phase margin 60˚ which is good enough for an OPAMP operating at a high frequency. A unity gain frequency of 2.2GHz is excellent for an OPAMP when all other parameters are also set at an optimized value.

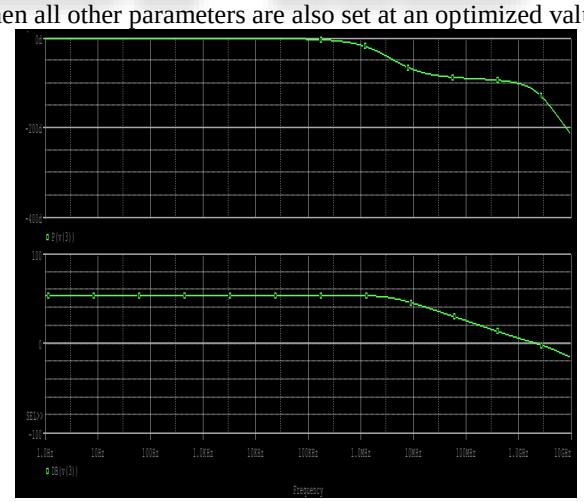

Fig. 3: Frequency response of the OPAMP

The slew rate simulation is carried out performing a transient analysis using a pulse waveform of 2V for a pulse period of 2us. The slew rate (+ve and –ve) are found to be 397V/us and 386V/us respectively, which is good as compared to other low power, low voltage OPAMPs. The slew rate response shown below-

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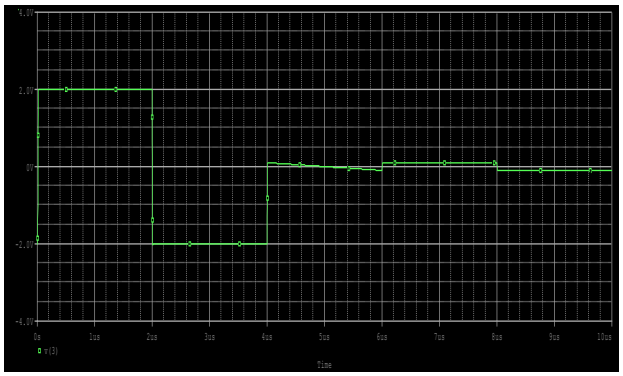

Fig. 4: Slew Rate (+ve and –ve) of OPAMP

The graph of the open loop transfer characteristic is shown below-

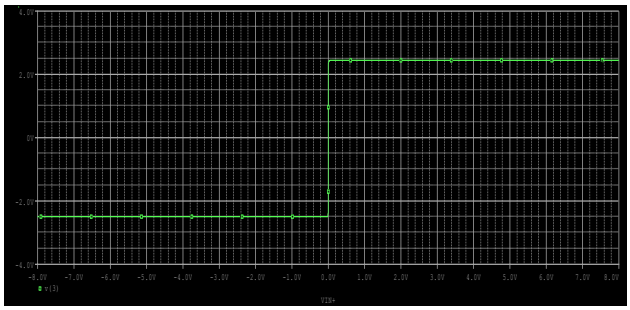

Fig. 5: Open loop transfer characteristic

The graph of input common mode range is shown below-

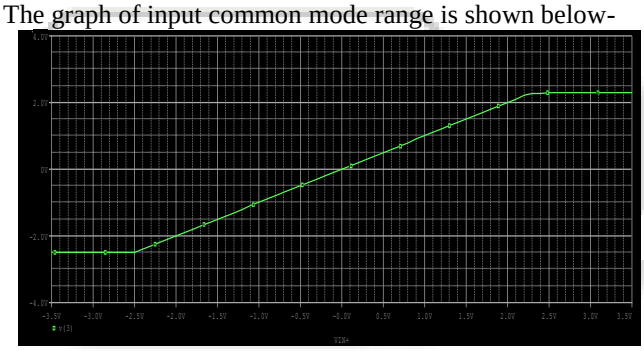

Fig. 6: Input common mode range of OPAMP

The Design Parameters		**The Electrical Parameters Yielded**	
M1	1.5/0.2 um/um	Phase margin	60˚
M2	1.5/0.2 um/um	Gain	54.11db
M3	3.2/0.4 um/um	C_C	30fF
M4	3.2/0.4 um/um	UGB	2.2GHz
M5	0.8/0.2 um/um	ICMR	-1.5V to 2.2V
M6	6.2/0.2um/um	Slew Rate(+ve)	397.5V/us
M7	1.2/0.2 um/um	Slew Rate(-ve)	386V/us
M8	1.4/0.2 um/um	CMRR	145db
M9	0.4/0.2 um/um	Common mode gain	-65db
I_{BIAS}	50uA	Power Dissipation	1.7mW
V_{DD}	2.5V	Output Resistance	16.6kΩ
C_L	10fF	3db frequency	1.17MHz

Table 1 The geometric dimension incorporated and the electrical parameter yielded

VI. CONCLUSION

An optimized compensation strategy for two stage CMOS OPAMP has been proposed for a high frequency OPAMP design. It is based on compensation of right half plane zero. A simple looking OPAMP design problem becomes harder one when it comes to optimizing all the parameters at a time. A careful analysis of circuit and deep insight into the circuit topologies and device operations leads to good implementation and desired result. The gain bandwidth product which is a constant puts challenges to the designers in designing the circuits for the high DC gain and high bandwidth applications. Here, the improvement in unity gain bandwidth has been done by increasing the bias current which decreases the DC gain and increases the power dissipation, still provides a good alternative control for an operational amplifier to operate at a high frequency.

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