Study and Review on Various Current Comparators

Vinod Kumar[1] Ms. Himani Mittal[2] Mr. Sumit Khandelwal[3]
[1]M. Tech. (VLSI Design) [2]Ph. D (Pursuing)
[1,2,3]Department of Electronics and Communication Engineering
[1,2,3]JSSATE, Noida, U.P., India)

Abstract— This paper presents study and review on various current comparators. It also describes low voltage current comparator using flipped voltage follower (FVF) to obtain the single supply voltage. This circuit has short propagation delay and occupies a small chip area as compare to other current comparators. The results of this circuit has obtained using PSpice simulator for 0.18 µm CMOS technology and a comparison has been performed with its non FVF counterpart to contrast its effectiveness, simplicity, compactness and low power consumption.

Key words: Current Comparator, Flipped Voltage Follower, Low Area Occupation, Low Voltage, Propagation Delay

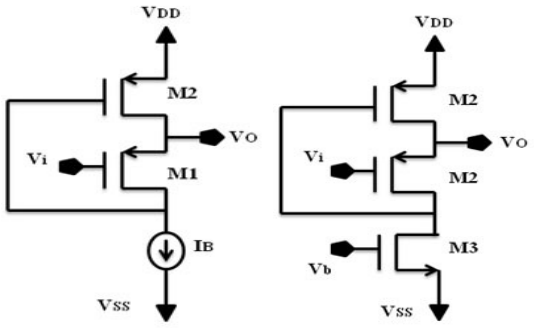
I. INTRODUCTION

Current comparator is a fundamental component of current-mode circuits. In recent years, current- mode circuits have become increasingly popular among analog circuits designers. This is mainly attributed to higher speed, larger bandwidth and lower supply voltage requirement compared to its voltage mode circuit counterpart. Current Comparator is widely used as a building block for analog systems including A/D converters, Oscillators and other signal processing applications. Many signal sources from temperature sensors, photo sensors generating very small current are required to be detected by low current comparators. Low voltage and low power application demands confront voltage mode IC designs, for there is less dynamic available under low power supply condition. While the circuit implemented in current mode technique occupies small area, consumes less power dissipation and achieves more dynamic range and high operation speed. Thus the current mode circuit design methodology receives increasing wide attention in the recent years. It is important that comparators are high speed, but if they are to be distributed across a processing array then they must also be low power. The process of downscaling of CMOS has been mainly driven by the need to reduce digital power supply consumption in mixed-mode VLSI systems.

They have always been, and are still, an important part of electronic systems. With the ever increasing need for shrinking the feature size of devices and the quest for high speed, designers are considering current-mode implementations. The very striking attributes of current-mode approaches such as high speed, large bandwidth, and decreased need of high supply voltages etc. have made analogue designers take more interest in current-mode circuits. The striking attributes of current-mode approaches such as high speed, large bandwidth, and decreased need of high supply voltages etc. have made analogue designers take more interest in current-mode circuits. Nowadays, where demand for portable battery operated devices is increasing, a major importance is given towards low power methodologies for high speed applications. Also we have to minimize the power consumption by using smaller feature size processes. The market of portable electronic equipment's has pushed industry to produce circuit designs with very low power consumption and with very low voltage supply. In order to accomplish both requirements it is necessary to develop new design techniques to reduce power consumption of the digital circuitry in VLSI systems and to prevent oxide breakdown with decreasing gate-oxide thickness. As the devices scale down, the supply voltage reduces while the threshold voltage of MOSFETs downscales not as much and the short channel effects become increasingly phenomenal. The crossfire of these factors diminishes the room for tradeoffs and hence toughens the design of a conventional source follower to meet the requirements of wide input swing and resistive load capability for the state-of-art circuits. Besides study on various current comparators this paper also describes a cell called Flipped Voltage Follower (FVF) which is a voltage follower circuit with shunt feedback hence the low impedance at the output node of the FVF facilitates large current sourcing capabilities [3]. The paper is organized as follows: The concept of FVF cell and its applications are presented in Section II. Section III describes literature survey of various current comparator configurations while Section IV elaborate current comparator structures, Comparison table. Finally, in Section V, conclusions are drawn.

II. FLIPPED VOLTAGE FOLLOWER

FVF is basically a Source Follower with shunt feedback and current/voltage biasing as can be seen from Fig. 1. Because of the shunt feedback, transistor M2 remains always in active state no matter how small power supply is given to the circuit. Thus the application of the shunt feedback extracts the whole circuit from saturation state to the active state.



(a) (b)

Fig. 1: (a) FVF using current bias (b) FVF using voltage bias [2]

The current through transistor M1 is held constant, due to current biasing. This change in output current does not affect the input current and V_{SG1} (which is a function of input current) remains almost constant across transistor M1. This result is almost unity voltage gain or in other words output voltage follows input voltage. Unlike the conventional voltage follower, the circuit in Figure 1(a) is

capable to source a large amount of current, but its sinking capability is limited by the biasing current source I_B, the large sourcing capability is due to the low impedance at the output node ($r_0=1/g_{m1}\ g_{m2}\ r_{01}$), where g_{mi} and r_{0i} are the transconductance and output resistance, respectively. This value is in the order of 20-100 Ω.

III. Literature Survey

A. J. Ramirez-Angulo et all

In this paper a cell called "Flipped Voltage Follower" has been revisited. It has been shown to be a useful cell with many applications in low-power, low-voltage analog design. Several new cells that exploit its class AB behavior in low-power, low-voltage operation have been also presented.

B. Lu Chen, Bingxue Shi and Chun Lu

A robust high-speed and low-power continuous-time CMOS current comparator have designed, whose delay time is comparable to existing fast current comparators.
Because of its lower power consumption, its speed/power ratio is better than those of other comparators. The simple structure and process robustness also make this circuit suitable to real applications.

C. D. Banks and C. Toumazou

A current comparator design has presented which is low power, operating in the 10s of Nano watts region and has accuracy to Pico ampere input currents. The DC power dissipation excluding the input bias currents is in the femtoampere region and the speed of operation is comparable to previous high-speed designs.

D. Soheil Ziabakhsh

have proposed an improved current comparator for high speed and low-power applications. in the proposed comparator, the power-delay product has been significantly reduced at low input current level in comparison with other reported comparators.

E. X. Tang and K.-P. Pun

A new high-performance current comparator based on Traff's circuit has presented. It achieves a much faster speed at low input current levels. With little circuit overhead introduced, the comparator also achieves low input impedance and is suitable for low voltage operation. Verified by transistor-level simulations, the proposed comparator can be used as an essential building block for a variety of current-mode systems, such as data converters and other front-end signal processing applications.

F. Ms. Rockey Choudhary et all

have presented a balanced low input impedance continuous-time CMOS current comparator. To deal with this problem, we utilize common-gate input stage and additional common-source negative feedbacks to effectively reduce the input impedance.

G. P. Iswerya et all

have presented an improved current comparator using flipped voltage follower (FVF) to obtain the single supply voltage. This Current comparator has short propagation delay and occupies a small chip area.

H. Hongchin Lin, et all

Have presented a high-speed low current comparator with low input impedance using a simple biasing method to achieve low input impedance and high gain In addition to less transistor number, the performance is better than most of the comparators in terms of the speed, power, sensitivity and the process tolerance for very low input current.

IV. Current comparator structures [1]

This section focuses on a current comparator using a flipped voltage follower to harness the potential of FVF cell for the design of high-performance low-power/low voltage analog and mixed-signal circuits. The input stage in [5] is replaced by a FVF Source follower cell which works on 1.8V power supply.

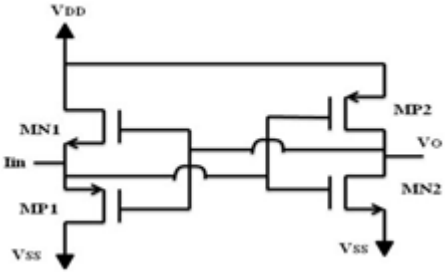


Fig. 2: Traff Current Comparator

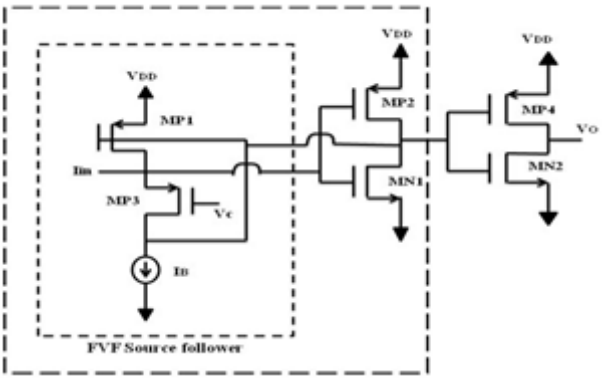


Fig. 3: FVF based Current Comparator

This FVF based current comparator structure employs only one additional CMOS inverter stage leading to a low transistor count as opposed to the modified Traff current comparator, which requires four stages.

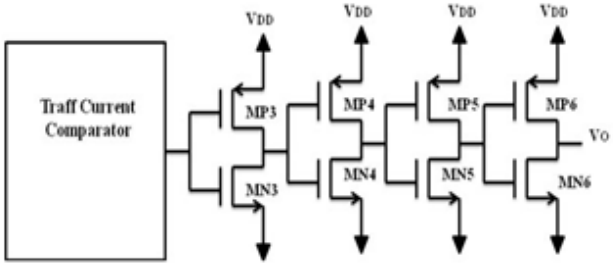


Fig. 4: Modified Traff current comparator (with output stages added to obtain full swing)

The modified Traff current comparator structure has 4 inverter stages at the output, for amplification purpose to obtain a complete output swing. In contrast, the Traff comparator gives a complete output swing when 4 inverter stages are added at the output as illustrated in Fig. 4.

	Power Supply(V)	Delay(ns)	Technology(um)	Transistor Count
Ms. Rockey Choudhary	3.3	40	0.35	27
D. Banks	3	14	0.35	8
Traff	3	10	2	6
Hongchin Lin	3	2.8	0.35	14
Varakorn kasemsuwan	3	1.02	0.50	15
P.Iswerya	1.8	0.75	0.18	6
Soheil Ziabakhsh	1.8	0.7	0.35	12
X.Tang	1.8	0.6	0.18	14

Table 1 Comparison of Various Current Comparators

V. CONCLUSION

The purpose of this paper is twofold. First, a literature survey on various current comparators, Second, for a current comparator using FVF with voltage output is presented, which exhibits low voltage, a short propagation delay of 0.75 ns and a relatively small area occupation.

A comparison of the performance with different current Comparators has also been drawn at TABLE 1. It can be seen from the above table that FVF based current comparator gives better results from other current comparators in terms of propagation delay, transistor count, power supply and technology used.

REFERENCES

[1] P. Iswerya, Student Member, *IEEE*, Shruti Gupta, Mini Goel, Veepsa Bhatia, Neeta Pandey and Asok Bhattacharyya, "Delay Area Efficient Low Voltage FVF Based Current Comparator", 978-1-4673-0455-9/12/$31.00 ©2012 IEEE

[2] Ms. Rockey Chaudhary, Ms.Monika Bhardwaj, Prof. B.P.Singh, Ms. Komal Gupta, "Design of Low Power Low Input Impedance CMOS Current Comparator", 2012 Second International Conference on Advanced Computing & Communication Technologies, 978-0-7695-4640-7/12 $26.00 © 2012 IEEE

[3] Carvajal, R., Ramirez-Angulo, J., Lopez Martin, A., Torralba, A., Galan, J., Carlosena, A., et al. (2005), "The flipp ed voltage follower: A useful cell for low voltage low power circuit design", IEEE Transactions on Circuits Systems I, 52(7), 1276–127 9. doi:10.1109/TCSI.2005.851387.

[4] Freitas, D. A. and Current, K. W., "CMOS curren t comparator circuit", Electron. Left., 1983, 19, pp. 695-697

[5] H.Traff, "Novel approach to high speed CMOS current comparator", Electronics Letters, Vol. 28, No. 3, pp. 310-312, 1992

[6] Soheil Ziabakhsh1, Hosein Alavi-Rad, Mohammad Alavi-Rad, Mohammad Mortazavi, "The Design of a Low-Power High-Speed Current Comparator in 0.35-µm CMOS Technology",10th Int'l Symposium on Quality Electronic Design.

[7] Hongchin Lin, Jie-Hau Huang And Shyh-Chyi Wong, "A Simple High-Speed Low Current Comparator" Iscas 2000 – Ieee International Symposium On Circuits And Systems, May 28-31, 2000, Geneva, Switzerland.

[8] [8] Varakorn kasemsuwan and Surachet Khucharoensin, "High Speed Low Input Impedance CMOS Current Comparator",Ieice Trans. Fundamentals,Vol.E88-A No.-6,June 2005.

[9] X. Tang and K. P. Pun, "High Performance CMOS Current Comparator", Electronics Letters, Vol. 45, No. 20, pp. 1007 – 1009, 2009.

[10] D. Banks and C. Toumazou, "Low-power high-speed current comparator design", Electronics Letters, 44, (3), pp. 171–172, 2008.

[11] S. S. Rajput and S. S. Jamuar, "Low voltage ana log circuit design techniques," *IEEE Circuits Syst. Mag.*, vol. 2, no. 1, pp. 24–42, May 2002.

[12] Traff and Holmbertg, "A CMOS current comparator ", Report LiTHISY- 1-1275, 1991

[13] C. Toumazou, F. J. Lidgey, and D. G. Haigh, Eds., "Analogue IC Design: The Current-Mode Approach", London, U.K.: P eter Peregrinus, 1990.

[14] Maneesha Gupta, Prashant Aggarwal, Pritender Singh, Naveen Kumar Jindal,"Low voltage current mirrors with enha nced bandwidth", Analog Integr Circ Sig Process (2009) 5 9:97–103 DOI 10.1007/s10470-008- 9241-2.

[15] Koliopoulos, C., & Psychalinos, C. (2007), "A c omparative study of the performance of the flipped voltage follower based low voltage current mirror", IEEE International Symposium on si gnals, Circuits and Systems, 1, 1–4 (Romania)

