A high accuracy, Low power, Reproducible temperature telemetry System
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Abstract— Sense amplifiers are extensively used in memory. Sense amplifiers are one of the most vital circuits in the periphery of CMOS memories. We know that memory is the heart of all digital systems. Today all worlds are demanding high speed and low power dissipation as well as small area. We know that speed and power dissipation of memory is overall depends upon the sense amplifier we used and their performance strongly affects both memory access time, and overall memory power dissipation. So it is important to design a good sense amplifier which performs well in both speed and power dissipation. In this dissertation, an implementation of a most efficient sense amplifier is done by comparing the best known sense amplifier in today. The dissertation focuses on design, simulation and performance analysis of sense amplifiers. In this thesis, current latch sense amplifier and body bias controlled current latch sense amplifier are designed and results compared. The result shows that the body bias controlled current latch sense amplifier is performing best. The result also shows a novel sense amplifier which consumes small power at same time its speed is faster than other sense amplifiers.

Keywords: CMOS, memory access time, SRAMs

I. INTRODUCTION

Digital system design in an amazing and emerging field now days. Each and every digital system has adequate memories. In memory today the CMOS memories are used in a much greater quantity than all the other types of semiconductor integrated circuit. SRAMs are used as large caches in microprocessor cores and serve as storage in various inputs on a system-on-chip like graphics, audio, video and image processors. SRAMs also used in high performance microprocessors and graphics chips so for each generation to bridge the increasing divergence in the speeds of the processor and the main memory we need high speed requirements. At the same time, SRAMs used in application processors which go into mobile, handheld and consumer devices have very low power requirements. So power dissipation has become an important consideration both due to the increased integration and operating speeds, as well as due to the explosive growth of battery operated appliances. As with other integrated circuits today, CMOS memories are required to increase speed, improve capacity and maintain low power dissipation.

To read the contents of this memory a sense amplifier is used. The sense amplifier converts the arbitrary logic levels of bitlines to the digital logic levels which required running the peripheral Boolean circuits of outside world of memory. In the SRAM data path, switching of the bitlines, I/O lines and biasing the sense amplifiers consume a significant fraction of the total power. Mainly performance of memory depends on the performance of SA such as delay and power dissipation.

So the sense amplifier is one of the most circuits in the periphery of CMOS memories. Speed and power dissipation of the memory is mainly depends on types of sense amplifier used. So performance of SA strongly affects both memory access time, and overall memory power dissipation.

II. SENSE AMPLIFIER

A sense amplifier is an active analog circuit that reduces the time of signal propagation from an accessed memory cell to the logic circuit located at the periphery of the memory cell array, and used to detect small variation on bitlines of memory and produce full voltage swing it means that converts the arbitrary logic levels occurring on a bitline to the digital logic levels of the peripheral Boolean circuits. The sense amplifier circuit has to operate within the conditions which are set by the operation margins. Operation margins in a digital circuit are those domains of voltages, current and charges. These domains unambiguously represent data throughout the entire operation range of the circuit. Operation margin depends on the circuit design, processing technology and environmental conditions. Sense amplifiers, used with memory cells, are key elements in defining the performance and environmental tolerance of CMOS memories. Because of their great importance in memory designs, sense amplifiers became a very large circuit-class. CMOS memories are used in a much greater quantity than all the other types of semiconductor integrated circuits, and appear in an amazing variety of circuit organizations.

\[
A_{d} = -g_{m} r \left( r_{L} \right) \left[ R_{L} \right]
\]

\[
A_{C} = \left( -g_{m} \left( r_{L} \right) \left[ R_{L} \right] \right) \left/ (1 + 2 g_{m} R_{S}) \right.
\]

\[
\Delta V_{o} = -2 \left( r_{d} \left[ R_{L} \right] \left( V_{d} - V_{S} \right) - V_{T} \left( V_{d} \right) \right) \Delta V_{i}
\]

III. IMPLEMENTATION AND SIMULATION OF SENSE AMPLIFIERS

As previously discussed in chapters about various sense amplifiers, it is found that some sense amplifier consume less power but with more delay than other consume slightly more power but speed (with less delay) is relatively large. In this dissertation I propose a new sensing scheme which has less delay, more sensitivity than previously discussed with less power consumption. This chapter divided into four parts.

- Current latch sense amplifier
- Latch operation
- The Sizing Consideration
- Body-biased controlled Current latch sense amplifier
These sense amplifiers made using with the help of Tanner tool V13.1.

IV. CIRCUIT CONFIGURATION

It consists of 5 nMOS and 4 pMOS transistors namely MN1, MN2, MN3, MN4, and MN5.

Fig. 1: Current Latch Sense Amplifier (CLSA)

Fig. 2: Current Latch Sense Amplifier (CLSA) with different W/L ratio

V. SIMULATION RESULTS

Fig. 3: Simulation waveforms of the Current Latch Sense Amplifier (CLSA) (a) for Bit Voltage (b) For Constant Voltage Difference

VI. CONCLUSION AND FUTURE SCOPE

In this chapter I summarize the conclusion for the proposed design and also explained about future scope.

A. Conclusion

In this dissertation Body Bias Controlled Current Latch Sense Amplifier has been designed and simulated using 180nm CMOS technology of Tanner tool at a various supply voltage from 1.0V to 5.0V. A Sense Amplifier is specially proposed in this dissertation as it is the heart of the Memory. Especially I proposed a BB-CLSA for low power and high speed operations in SRAM. This proposed Sense amplifier is compared with nearest basic Current Latch Sense amplifier as

- The power consumption of proposed BB-CLSA has been reduced from 47% to 87% compared to conventional CLSA.
- Speed of proposed Sense amplifier is increased by 10% as compared to conventional CLSA.
- Noise Margin and Sensitivity of proposed sense amplifier is improved considerably.
- Body Bias method is used for high speed at low power dissipation operation.
- Only 44% more transistors are used to reduce about 87% power dissipation and to get 10% more high speed operation.

B. Future Scope

However some aspects of the goal have been achieved using this design, but still a better Sense Amplifier can be build by some improvement in the circuit design. The SA can be further extended and modified by the following points.

- Delay can be further reduced by improving circuit design.
- Affect of process variations and corner variations on the performance of the proposed sense amplifiers are not included. So effects of these variations are removed by proper design of circuits and accurate simulations.
- Yield measurements can be done
- The layout can also be designed using L-Edit of Tanner tool by which area can be calculated for chip fabrication.
- Body Bias Voltage Latch Sense amplifier is designed for high speed operation.
- In this design we use 180 nm technologies but latest technology 28nm and more can be used for batter design and analysis.
- The layout can also be designed using L-Edit of Tanner tool by which area can be calculated for chip fabrication
- The delay and power dissipation can also reduced by using low power and high speed techniques like VTCMOS, DTCMOS, and Adaptive CMOS and Adiabatic logic technology.

Table 1: CLSA operation

<table>
<thead>
<tr>
<th>Vsae</th>
<th>Vbl</th>
<th>Vblb</th>
<th>Vout</th>
<th>Vouth</th>
<th>Remark</th>
</tr>
</thead>
<tbody>
<tr>
<td>5V</td>
<td>5V</td>
<td>4.5V</td>
<td>0V</td>
<td>5V</td>
<td>In sense mode</td>
</tr>
<tr>
<td>0V</td>
<td>5V</td>
<td>4.5V</td>
<td>5V</td>
<td>5V</td>
<td>In pre-charge mode</td>
</tr>
</tbody>
</table>
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