

# A Sub-1-V 15-ppm/ C CMOS Band Gap Voltage Reference

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**Abstract**— A sub-1-V CMOS band gap voltage reference requiring no low threshold voltage device is introduced in this paper. In a CMOS technology with  $v_{thn}=v_{thp}=0.9\text{ V}$  at  $0\text{ C}$ , the minimum supply voltage of the proposed voltage reference is  $0.98\text{ V}$ , and the maximum supply current is  $18\text{ A}$ . A temperature coefficient of  $15\text{ ppm/ C}$  from  $0\text{ C}$  to  $100\text{ C}$  is recorded after trimming. The active area of the circuit is about  $0.24\text{ mm}^2$ .

**Key words:** CMOS band gap voltage reference, low voltage, temperature

## I. INTRODUCTION

LOW VOLTAGE and low power are two important design criteria in both the analog and digital systems. It is expected that the whole system will be able to operate down to a single 1-V supply in the near future. A voltage reference, as one of the core functional blocks in both analog and digital systems, should be able to operate from a single 1-V supply for both systems. In CMOS technology, a parasitic vertical bipolar junction transistor (BJT) formed in a p- or n-well is commonly used to implement a bandgap reference [1]–[3]. The minimum supply voltage needs to be greater than 1 V due to two factors: 1) the reference voltage is around 1.25 V which exceeds 1-V supply [4], [5] and 2) low-voltage design of the proportional-to-absolute-temperature (PTAT) current generation loop is limited by the common-collector structure of the parasitic vertical BJT [2] and the input common-mode voltage of the amplifier [4], [6]. The first problem can be solved by resistive subdivision methods [7], [8] to scale down the 1.25-V reference voltage. The second problem can be solved by using BiCMOS process [6] or by using low threshold voltage devices [7], [8]. As shown in Fig. 1(a), the minimum input common-mode voltage of an amplifier with an nMOS input stage must be less than one  $V_{EB(on)}$  which implies that  $V_{thn} < 0.6\text{ v}$  is required (assuming  $V_{EB(on)}=0.7\text{ v}$  and  $V_{ds(sat)}=50\text{ mv}$ ) This is acceptable as nMOS transistors with  $V_{thn} < 0.6\text{ v}$  can be easily found in many technologies. However, the temperature effect on the base-emitter voltage and threshold voltage should be considered. The temperature coefficient (TC) of the base-emitter voltage is approximately  $2\text{ mV/K}$  [9] while that of the threshold voltage of the nMOS transistor may be greater than  $-2\text{ mV/K}$ . To address the above-mentioned design problems, a sub-1-V bandgap reference circuit in a standard CMOS process is presented in this paper. The key feature of the proposed reference circuit is that no low threshold voltage device is needed. The design techniques for achieving a good performance are also presented in detail.

## II. PROPOSED SUB-1-V BAND GAP VOLTAGE REFERENCE IN CMOS TECHNOLOGY

The structure and the complete schematic of the proposed

Sub-1-V band gap voltage references are shown in Figs. 2 and 3, respectively. The reference core circuitry is modified from the one proposed by Banba *et al.* [7]. The main differences are that an amplifier with a pMOS input stage is used and the inputs of the amplifier are connected to nodes N1 and N2 instead of nodes N3 and N4. A self-bias approach is used in this circuit to bias the amplifier. The compensation capacitor  $C_b$  [11] is used to stabilize the reference. A larger  $C_b$  provides better stability, but the startup time will be longer. As illustrated in Fig. 2, the amplifier enforces nodes N1 and N2 to have equal potential. As a result, nodes and also have the same potential when  $R2A1=R2B1$  and  $R2A2=R2B2$ . Therefore, the loop formed by Q1, Q2, R1, R2A1, R2B1 and generates a current given by  $I=V_{EB2}/R2+V_T \cdot \ln N/R1$

Where  $N$  is the emitter area ratio, is the thermal voltage, and  $R2=R2A1+R2A2=R2B1+R2B2$ . The current is injected to  $R3$  by the current mirror formed by M1, M2, and M3, and this gives the reference voltage as follows:  $V_{ref}=R3/R2 \cdot [V_{EB2}+(R2/R1 \ln N) \cdot V_T]$ .

A scaled-down band gap reference voltage can be obtained by an appropriate resistor ratio of  $R3$  to  $R2$ . Moreover, trimming

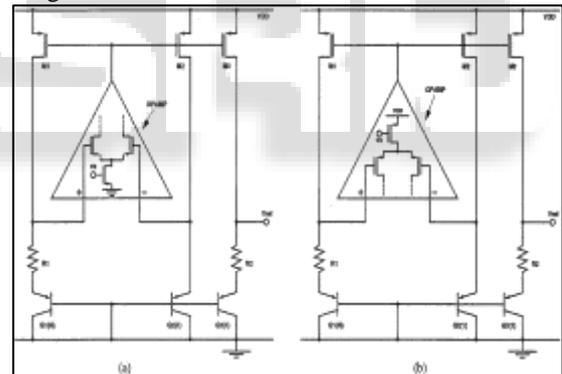


Fig. 1: Band gap voltage references in CMOS technology using an amplifier with (a) nMOS input stage, and (b) pMOS input stage.

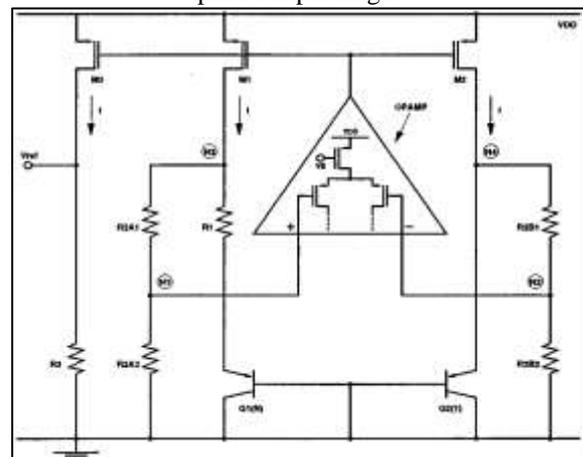


Fig. 2: Proposed sub-1-V band gap voltage reference.

On the resistor ratio (ratio of R2 to R1) to achieve a good TC can be done on R2A1 and R2B1 simultaneously. When the sum of the voltages across R2B1 and R2B2 (or R2A1 and R2A2 ) is equal to VEB2 , the voltage with respect to ground at N1 and N2 is  $(R2B2/R2B1+R2B2) \cdot VEB2$ . Therefore, the minimum supply voltage  $V_s$  , which should be evaluated at the lowest operating temperature, is given by  $V_s(\min)=(R2B2/R2B1+R2B2) \cdot VEB2+V_{thp}+2 \cdot V_{DS}(\text{sat})$ . The minimum supply voltage is substantially reduced when  $(R2B2/R2B1+R2B2) \cdot VEB2$  is set to a small value. This structure is suitable for any CMOS technology to implement low-voltage bandgap reference.

#### A. Operation in High-Gain Region by Forward Biasing the Source–Bulk Junctions of pMOS Transistors

A high-gain amplifier with ultralow offset voltage is very important in the proposed bandgap reference to ensure that the nodes N1 and N2 in Fig. 2 have nearly the same potential. However, as the output of the amplifier is connected to the gates of pMOS transistors (M1, M2 and M3), the amplifier may not operate at the high-gain region [6]. As shown in Fig. 4, the operating point of the output of the amplifier is  $V_{DD}-V_{GSP}$  . If the supply voltage is low, for example, 1 V, this node voltage of the output of the amplifier may be close to the ground, and this enforces the nMOS transistor of the output stage to operate in triode region (region A in Fig. 4). As a result, the gain of the amplifier is reduced severely. A method to reduce the threshold voltage of the pMOS transistors is to forward bias the source–bulk junction [12] since the threshold voltage of a pMOS transistor is given by [9], [12] In [12], the forward-biased junction is defined by the voltage drop across a Schottky diode. In order to eliminate the use of the Schottky diode and allow the reference circuit to be compatible to any CMOS process, a temperature-independent voltage across RSB, as shown in Fig. 3, is needed. This voltage is generated by drawing the current given by (1) from MSB, and the voltage across RSB is used to forward bias the source–bulk junctions of all pMOS transistors. The temperature-dependent bulk

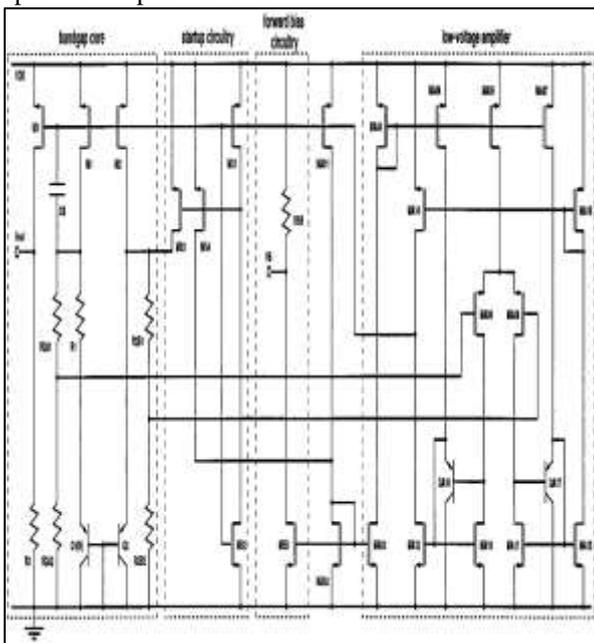


Fig. 3: Complete schematic of the proposed sub-1-V band gap voltage reference (the source–bulk junctions of all pMOS transistors are forward biased by V except MA08 and MA09).

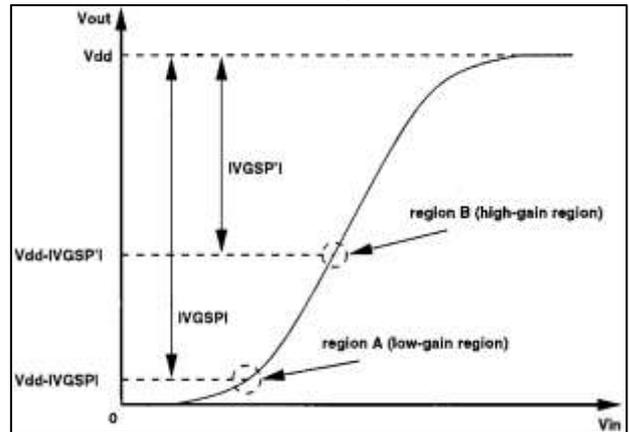


Fig. 4: Transfer characteristic of the low-voltage amplifier

Current injected to VB is small compared with the bias current drawn from MSB. As a result, the voltage across RSB is not exactly temperature independent but decreases slightly according to temperature. Thus, the maximum forward bias voltage is set to about 0.3 V at the lowest operating temperature to avoid turning on the p–n junction between the p-substrate and n-well.

### III. COMPARISON WITH OTHER REPORTED LOW-VOLTAGE BAND GAP REFERENCES

A comparison with other reported low-voltage bandgap references is tabulated in Table I. From the table, technologies with low  $V_{thn}$  are required in [4] and [8] while native nMOS transistors are needed in [7]. DTMOST is used in [5], and BiCMOS process is used in [6]. The main reason for these approaches is to overcome the problem of the input common-mode voltage of the error amplifier in the PTAT current generation loop. However, the proposed reference can solve this problem with sub-1-V supply operation and provide comparable performance on TC.

### IV. CONCLUSION

A 0.98-V 15 ppm/ C CMOS band gap voltage reference, which consumes a maximum of 18 A at 1.5-V supply and 100 C, has been presented. The main features are that no low threshold voltage device is needed and thus the circuit is reproducible in any CMOS technology. If low threshold voltage pMOS transistors  $V_{thp} < 0.65$  ( V) are used, the minimum supply voltage can be reduced to about 0.75 V  $VEB+V_{DS}(\text{sat})$ . In addition, techniques to achieve sub-1-V operation, such as reducing the threshold voltages by forward biasing the source–bulk junctions, improving the lower common-mode input range of the amplifier by dc level shifting current mirrors, and low-voltage startup circuits for self-biased voltage reference, have been described.

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