Design and Analysis of a Low Power High Performance Circuit for Dynamic CMOS Logic

Suminder Kaur[1] Er. Rajni[2]
[1]M.Tech Student
[1,2]Department Electronic & Communication Engineering
[1,2]JCDMCOE, Sirsa, Haryana

Abstract— Dynamic logic is highly applicable due to its high performance and fast speed. The requirement of number of transistors decreases eminently in dynamic logic as compared to the CMOS logic so it is more efficient than the CMOS logic. In this paper we have proposed a domino circuit for low power consumption and very less power delay product. The results and their comparison to the previous design are given at the end of the chapter. The chapter is divided into different sections starting from discussion about the tool and language used, after that the next section presents the proposed work and results. The last section compares the proposed design with existing designs of d-CDMFF.

Key words: CMOS, VLSI, PDN, VERILOG-A

I. INTRODUCTION

The rapid advancement in VLSI circuit is due to incremented utilization of portable and wireless systems with low power budgets and microprocessors with higher speed. To achieve this, the size of transistors and supply voltages are scaled down along with technology. Due to more sizably voluminous number of contrivances per chip the interconnection density increases. The interconnection density along with high clock frequency increases capacitive coupling of the circuit. Therefore, noise pulses kenned as cross-verbalize are engendered leading to logic failure and delay of the circuit. Again, when supply voltage is scaled, threshold voltage of the contrivance needs to be scaled to preserve the circuit performance, which in turn leads to increment in the leakage current of the contrivance. Due to high speed and low contrivance count especially compared to complementary CMOS, dynamic-logic circuits are utilized in a wide variety of applications including microprocessors, digital signal processors and dynamic recollection. Dynamic circuit contains a pull-down network (PDN) which realizes the desired logic function. According to the rudimentary theory, the dynamic logic circuit will precharge at every clock cycle. Due to the high frequency of the clock signal a plethora of extra noise is introduced in the circuit that consumes adscititious power and decelerates the circuit.

In this paper we propose an incipient circuit technique which can reduce the noise of dynamic logic dramatically. This circuit increases speed and decreases the potency dissipation of the circuit as compared to other domino logic styles.

II. ANALYSIS OF THE DOMINO CIRCUIT

The tool provides a complete schematic capture and editing option with a support to netlist and VERILOG-A files, which can be used to import designs from different tools. The tool provides a graphical user interface which makes schematic capture easy and convenient. The captured schematic is used by tool to automatically generate the SPICE code which is further used by T-SPICE for simulation process. The tool supports models of different levels and technologies. Snapshots of different windows of the tool are given below in fig 4.1 and 4.2. The first figure shows the workspace in the tool. The libraries are present on the left and property window on the right. At center the grid is present. Below the grid is the command window. The next snapshot shows an example of design and the simulation setup window in the tool.

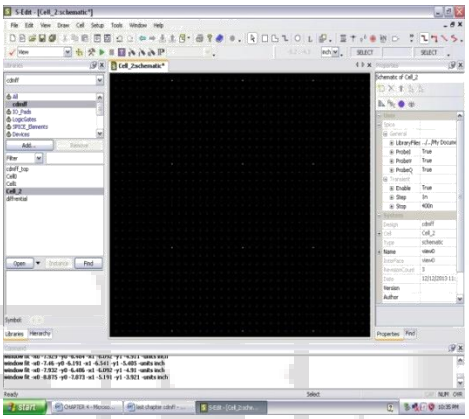

Fig. 1: Snapshot of workspace of S-EDIT

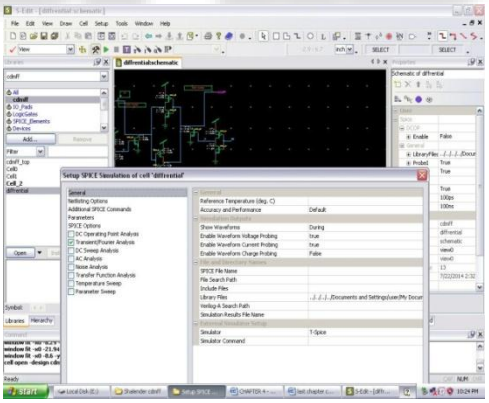

Fig. 2: Snapshot of a design and simulation setup

A. T-SPICE:

It generates the simulation code for the program. With the help of T-SPICE command, we can calculate exact result of current, power dissipation and delay in the circuit.

III. PROPOSED WORK

In the present work we have worked on optimization of dynamic comparator using different techniques. The proposed design has been modified in two aspects. The design of dynamic comparator has been optimized to obtained low area and fast simulation of given design. Here

we are using 0.5-1GHz frequency at 2V supply voltage and 90nm-CMOS technology. In new design, we have used the concept of XOR gate to compare the input signals. So it reduces power consumption in the circuit. Using this technique, we have developed 1-bit, 2-bit and 4-bit dynamic comparator.

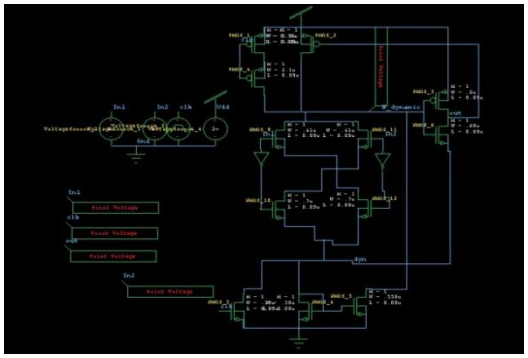

Fig. 3: Schematic of a new 1-bit dynamic comparator design

Using T-SPICE, we calculated the average power consumed and delay [from 50% of input data (D) to 50% of output data (Q)] in the circuit.

We know that power consumed (dynamic power dissipation) by circuit is given by

$$P = C.Vdd^2.f$$

where C is the load capacitance, Vdd is power supply and f is the frequency of operation.

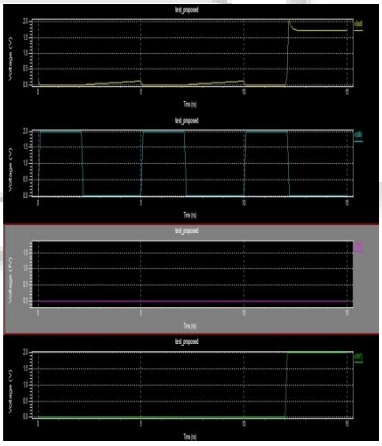

Fig. 4: Waveform of a new dynamic comparator design

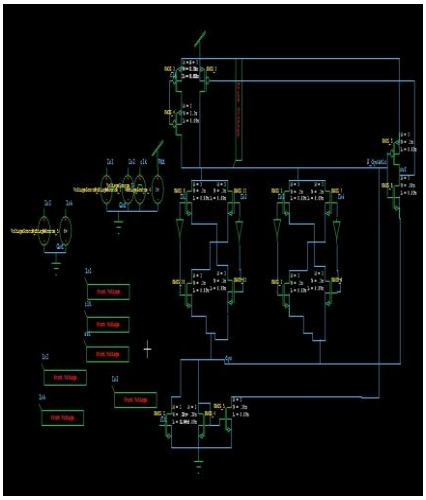

Fig. 5**:** Schematic of a new 2-bit dynamic comparator design

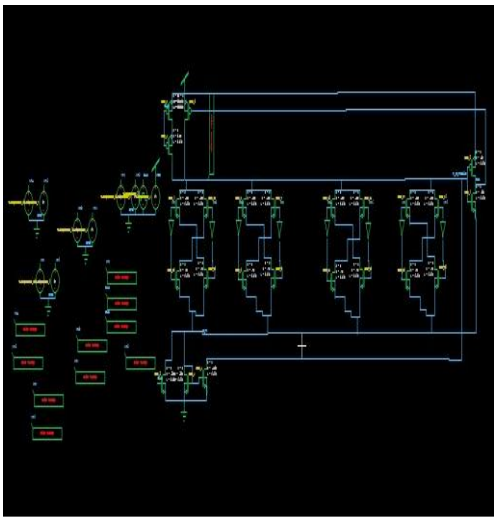

Fig. 6**:** Schematic of a new 4-bit dynamic comparator design

A. Comparison Table of the previous and proposed dynamic comparator:

Comparator_fan-in	Parameter	Scheme in Paper	Proposed Circuit
1-bit	Delay	4.19 E -11	4.99 E -11
	Power (Avg) α=100%	4.11 uW	2.09 uW
	Max. Freq.	200 MHz	0.5-1 GHz
2-bit	Delay	5.13 E -11	6.34 E -11
	Power (Avg) α=100%	7.99 uW	4.29 uW
	Max. Freq	200 MHz	0.5-1 GHz
4-bit	Delay	7.01 E -11	7.89 E -11
	Power (Avg) α=100%	8.11 uW	7.98 uW
	Max. Freq.	200 MHz	0.5-1 GHz

IV. CONCLUSION

The optimization of the design was successful with decreasing the power consumption. The regressive approach has been used in this work where we have decreased power-delay product using separate comparison technique. The optimized design with new low PDP helps in increasing the speed of the comparator which is good for the high frequency applications. The obvious decrease in power consumption has been handled by the power reduction circuit and is proved in the results.

The proposed design is focused on reduction of static, dynamic and leakage power; it can be improved by

some applying techniques with voltage lowering. The design can be further optimized for size, power and delay for higher frequency applications.

REFERENCES

[1] F. Mendoza-Hernandez, M. Linares-Aranda and V. Champac, "Noise tolerant improvement in dynamic CMOS logic circuit", IEEE Proc.-Circuits Devices Systems, Vol 153, No. 6, Dec 2006, pp.. 565-573
[2] H.L. Yeager et al, "Domino Circuit Topology", U. S. Patent 6784695, Aug. 31, 2004.
[3] Mahmoodi-Meimand H., Roy K.: 'Diode-footed domino: a leakage-tolerant high fan-in dynamic circuit design style', IEEE Trans. Very Large Scale Integr. Syst., 2004, 51, (3), pp. 495–503
[4] F. Frustaci, P. Corsonello, G. Cocorullo: 'A new noise-tolerant dynamic logic circuit design', IEEE Ph.D. Research in Microelectronics and Electronics, PRIME 2007, Bordeaux, France, July 2007, pp. 61–64
[5] Fang Tang, Ke Zhu, Quan Gan and Jian Guo Tang, "Low-noise and power dynamic logic circuit design based on semi-dynamic logic", Anti-counterfeiting, Security and Identification, 2008. ASID 2008. 2nd International Conference on 20-23 Aug. 2008, pp
[6] F. Frustaci P. Corsonello S. Perri G. Cocorullo: 'High-performance noise-tolerant circuit techniques for CMOS dynamic logic", IET Circuit Devices Syst., Vol. 2, No. 6, pp. 537-548
[7] Kiat-Seng Yeo, Kaushik Roy, "Low-voltage low-power voltage subsystems" Tata Mc-Graw-Hill edition 2009

