Area-Efficient VLSI Implementation for Parallellinear-Phase FIR Digital Filters

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Abstract— To design an efficient integrated circuit in terms of Area, Power and speed is one of the challenging task in modern VLSI design field. In the past decade numbers of research have been carried out to optimize design based on area, speed and power utilization. In this paper performance analysis of different available adder architectures has been carried out and then we proposed a Heterogeneous architecture, which composed of four different sub adders to design an adder unit in order to demonstrate trade-offs between performance parameters i.e. Area, Power and speed. In proposed approach the symmetric coefficients of FIR filter area taken into consideration to implement parallel (L=3) FIR filter.

Keywords: - Heterogeneous Adders, Parallel FIR, Symmetric Convolution, Digital Signal Processing(Dsp)

I. INTRODUCTION

Along the growth of multimedia application, the demand for high-performance and low-power digital signal processing (DSP) is getting higher and higher. The FIR digital filter is one of the most widely used essential devices. Some applications need the FIR filter to operate at high frequencies such as video processing, whereas some other applications request high throughput with a low-power circuit such as multiple-input–multiple-output systems used in cellular wireless communication. Furthermore, when narrow transition band characteristics are required, the much higher order in the FIR filter is unavoidable. Parallel processing in the digital FIR plays key role. The hardware implementation cost of the parallel processing increases due to increase in block size L, hence parallel processing technique loses its advantage to be employed in practice.

Adders are most commonly used in various electronic applications e.g. Digital signal processing in which adders are used to perform various algorithms like FIR, IIR etc. The major challenge for VLSI designer is to reduce area, power and increase the speed of operation using efficient optimization techniques Speed of operation is one of the major constraints in designing DSP processors. Many parallel adders are studied where all the inputs are available before the start of the computation. The parallel adders which are selected for the project vary widely in their delay and speed characteristics. Since asynchronous systems are not very common, we concentrate on building synchronous adders for the paper.

The adders studied are linear time ripple carry adder, Ling adder, square-root time carry skip adder and logarithmic time carry look-ahead adder. These adders have their own benefits and limitations with respect to performance parameters e.g. implementing Ripple carry adder utilizes less area but at the cost of large delay, whereas, carry look-ahead adder gives delay efficient design but at the cost of large chip area requirement. Therefore, for efficient design various hybrid architecture were proposed by adopting a different scheme for carry and sum generation. In this project, new architecture is proposed that combine different types of adder to form a single heterogeneous adder to satisfy design constraints.

The adders presented here are all modeled by using VHDL for 16-bit unsigned data. XILINX ISE v 14.5i is used as synthesis tool and FPGA-Spartan VI (XC3S250E) device is selected to get area report. Model Sim XE III 6.2g is used to get timing simulation.

II. RELATED WORK

Yu-Chi Tsao and Ken Choiin [1] proposed a new parallel FIR filter architectures, which are beneficial to symmetric convolutions of odd length in terms of the hardware cost and which utilize the inherent nature of symmetric coefficients reducing half the number of multipliers in the sub filter section at the expense of increase in adders in preprocessing and postprocessing blocks. Multipliers weigh more compared to adders in case of hardware cost and speed.

Animesh Panda and Satish Kumar Baghmar [2] proposed that an FIR Filters can be designed using frequency sampling or windowing methods. The peak error can be computed using a computer-aided iterative procedure, known as the Remez Exchange Algorithm. This particular algorithm tremendously reduces the number of multipliers and adders being used.

FIR filter design based on low-voltage micro power asynchronous signed truncated multiplier which corresponds to shift-add multiplication approach is proposed in [3]. The emphases of the design are micro power operation and small IC area and high throughput. In the existing method, Wallace tree multiplier is employed to get the better efficiency. But in Wallace tree multiplier the power is reduced compared to other types of multipliers. The main drawback is the increase in area. In order to overcome the drawback, S. Karunakaran and Dr. N. Kasthuri simulated design of low-voltage micro power asynchronous multiplier using shift-add multiplication. In the proposed method the hardware complexity is reduced.

Sangeeta Mondal and S. P. Ghoshal proposed an optimal design of linear phase digital low pass finite impulse response (FIR) filter using Novel Particle Swarm Optimization (NPSO). NPSO is an improved particle swarm optimization (PSO) that proposes a new definition for the velocity vector and swarm updating and hence the solution quality is improved. The key feature of the proposed modified inertia weight mechanism in [4] is to monitor the weights of particles, which linearly decrease in general applications. FIR filter design is a multi-modal optimization problem. The simulation results clearly indicate that NPSO demonstrates the best performance in terms of magnitude

response, minimum stop band ripple and maximum stop band attenuation with the narrowest transition width.

Tanee Demeechai and Siwaruk Siwamogsatham [5] proposed a new architecture for decimating finite impulse response filters. The architecture is based on using a number of accumulators. The size of each accumulator can be minimized, depending on the filter coefficients. A demonstrative FPGA implementation shows that the new architecture utilizes less area with similar power consumption.

S. K. Saha and R. Choudhury [6] proposed that opposition-based harmony search has been applied for the optimal design of linear phase FIR filters. The original harmony search algorithm is chosen as the parent one, and opposition-based approach is applied. A comparison of simulation results reveals that OHS has the ability to converge to the best quality near optimal solution and possesses the best convergence characteristics in moderately less execution times among the algorithms.

Magatha Nayak Bhukya and K. Anjaiah [7] proposed detailed analysis and discussion in the algorithm, the memory size and the look-up table speed. **As** when the DA algorithm is directly applied in FPGA to realize FIR filter, it is difficult to achieve the best configuration in the coefficient of FIR filter, the storage resource and the computing speed. Aiming at the problems of the best configuration in the coefficient of FIR filter, the storage resource and the calculating speed, the DA algorithm is optimized and improved in the algorithm structure, the memory size and the look-up table speed.

III. PROPOSED WORK

The proposed 18-bit Heterogeneous adder in this project consists of four sub adders, namely

1. 4 bit Ripple carry adder(RCA) architecture,
2. 4-bit Carry select adder(CSA) architecture,
3. 6 bit and 4 bit carry look ahead(CLA) architecture respectively

All sub adders concatenates to form a heterogeneous adder.

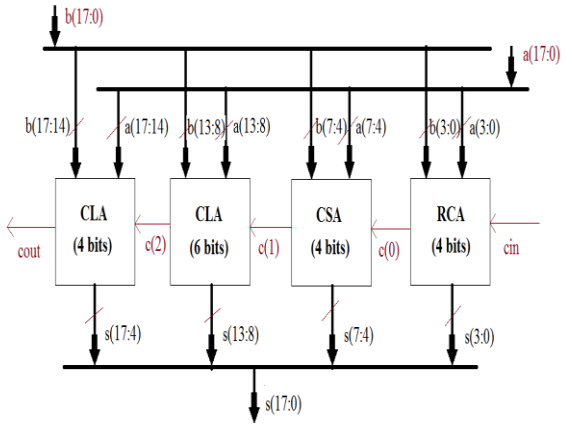

Fig. 1: 18-bit Heterogeneous adder

The order of sub adder has an impact on the performance of a heterogeneous adder. From the table 4.1 as shown below, it is observed that heterogeneous adder requires less area but at the cost of large delay. Therefore, in order to get optimized result in terms of area utilization and speed of operation three adders are combined to form a single adder with different bit size.

Table 1 shows that the proposed structure uses less area with almost same delay. Comparing the performance metrics for the 18-bit adders implemented on Xilinx FPGA board, using Synopsys synthesis tools, the trade-offs becomes apparent.

Table 1: Delay and area consumption of different adder

Parameters	**CSA (18 bits)**	**CLA (18 bits)**	**Heterogeneous (18 bits)**
Area	36 LUTs	35LUTs	34 LUTs
Delay	31.53 ns	28.76 ns	30.7 ns

As can be seen there exist an inverse relationship between time delays, operating speed, and circuit area, in this case the number of CLBs (measure of the area). The ripple carry adder, the most basic of flavors, is at the one extreme of this spectrum with the least amount of CLBs but the highest delay. The carry select adder on the other hand, is at the opposite corner since it has the lowest delay (half that of the ripple carry's) but with a larger area required to compensate for this time gain. Finally, the carry look-ahead is middle ground.

To make full use of symmetry of coefficients , polyphase decomposition is handled in such a way that earns as many as subfilter blocks that are possible, which contain symmetric coefficients so that half the number of multipliers within a single subfilter block can be utilized for the multiplications of whole taps.

3x3 Proposed FFA (L=3)

In figure.1 new three-parallel FIR filter structure is proposed which enables more multipliers sharing in the subfilter section. Therefore this can save more hardware cost over the existing FFA.

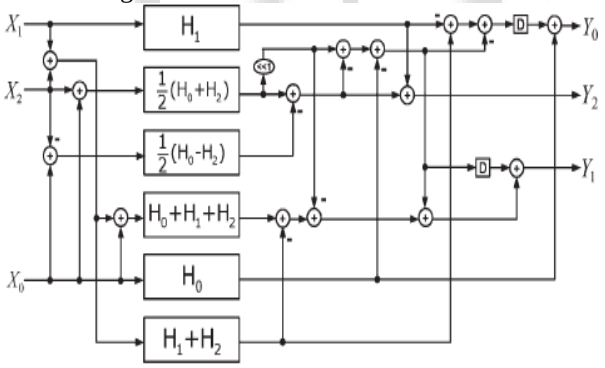

Fig. 2: Three-parallel FIR structure 3*A*.

The following equations correspond to the three parallel structure 3A:

$$Y_0 = H_0X_0 + z^{-3}\{(H_1 + H_2)(X_1 + X_2) - H_1X_1 - ((H_0 + H_2)(X_0 + X_2) - H_0X_0 - \frac{1}{2}[(H_0 + H_2)(X_0 + X_2) - (H_0 - H_2)(X_0 - X_2)]\}$$

$$Y_1 = (H_0 + H_1 + H_2)(X_0 + X_1 + X_2) - (H_1 + H_2)(X_1 + X_2) - (H_0 + H_2)(X_0 + X_2) + \Big\{(H_0 + H_2)(X_0 + X_2) - \frac{1}{2}[(H_0 + H_2)(X_0 + X_2) - (H_0 - H_2)(X_0 - X_2)] - H_0X_0\Big\} + z^{-3}\Big\{(H_0 + H_2)(X_0 + X_2) - \frac{1}{2}[(H_0 + H_2)(X_0 + X_2) - (H_0 - H_2)(X_0 - X_2)] - H_0X_0\Big\}$$

$$Y_2 = H_1X_1 + \frac{1}{2}[(H_0 + H_2)(X_0 + X_2) - (H_0 - H_2)(X_0 - X_2)]$$

In the proposed structure 3A, in Fig.2, four out of six subfilter blocks, i.e., H1, H0 ± H2, H0 + H1 + H2, are with symmetric coefficients now, which means a single subfilter block can be realized with only half the amount of multipliers required. Each of the multipliers responds to two taps except the middle filter. Here Transposed Direct-form FIR filter is used. Compared to the existing one, the proposed structure leads to two more subfilter blocks, which contains symmetric coefficients. However, in proposed structure there is increase in amount of adders, i.e., five additional adders, in preprocessing and postprocessing blocks.

IV. Result

In three parallel structure's sub filter block, multipliers are replaced with additional adders and substractor. Therefore, for an N-tap three-parallel FIR filter, the proposed structure can save N/3 multipliers from the existing FFA structure [8][9].

In the above comparisons we observed that number of adders is more compared to existing structure. Since multipliers are slow n major hardware consumption, they are replaced by adders. Adders are fast, low cost and less complex compared to multipliers. Hence it is profitable to exchange multipliers with adders.

Fig.3: ISIM-simulation of Heterogeneous Adder

The Simulations are done with the respective tools as mentioned. During this study we are able to observe that carry look-ahead adder has more delay so therefore we have implemented for heterogeneous adder, where we analyzed that there is comparable increase in speed. The proposed Parallel 3A structure using heterogeneous adder are coded in Verilog Hardware Description Language using structural modeling in Xilinx ISE Design Suite 14.5i and all the simulation results are verified using XILINX ISIM simulator. Synthesized for the Spartan-6FPGA XC3S400 with the speed grade of 2. Inputs are generated using Verilog HDL test bench.

V. Performance Analysis

Designing both the adders in the proposed 3A architecture, we can conclude that heterogeneous adder is faster than carry look-ahead adder since heterogeneous adders give less delay compared to carry look-ahead adder.

Parameters	**Carry Look-Ahead Adder**	**Heterogeneous Adder**
Delay	39.580ns	36.510ns
Number of LUTs used	39	0
Number of bounded IOBs utilization	62%	50%

Table 2: Comparison between Carry Look-Ahead Adder and Heterogeneous Adder

VI. Conclusion

Here a new parallel FIR filter structure is presented, which utilize the nature of symmetric convolution of odd length. Since multipliers are the major hardware consumption, the proposed method reduce the amount of multipliers required at the cost of additional adders. Compared to adders, multipliers weigh more in hardware cost.

To analyze trade-offs in designing digital adder, we proposed a heterogeneous adder architecture, which consists of sub-adders of various sizes and carry propagation schemes. The proposed architecture allows more design trade-offs and hence provide flexibility to optimize design as per application demand. In this project adder design has been optimized in terms of hardware (Area) utilization and speed of operation.

The proposed structure i.e. heterogeneous adders are used in new parallel FIR filter structure 3A which is obtained by polymorphic decomposition of basic FIR design which results in less delay and area in hardware point of view.

Therefore, heterogeneous adders give less delay when compared to carry look-ahead adders.

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