FPGA Implementation of Efficient 16-Bit Parallel Prefix Kogge Stone Architecture for Convolution Applications

Geetha.B[1] Ramachandra .A.C[2]
[1]4th SEM, M.Tech Dept. of ECE [2]HOD & Professor Dept. of ECE
[1, 2] ACE, Bangalore

Abstract— Adders form important parts of any digital circuits. Adders are much used in all integrated digital circuits because any process involving multiplication and any binary functions use adders in their processes. Adders are not only necessary for addition, but it also needs for other parameter such as subtraction, multiplication and division. In this paper we have proposed both kogge stone adder and carry select adder. The proposed adder is synthesized using Spartan 3s400-tq144. A comparative study of delay of kogge stone adder and carry select adder were analyzed and shown that delay has been reduced in kogge stone adder compared to that of carry select adder.

Keywords: - carry select adder, kogge stone adder,circuit delay,convolution

I. Introduction

Adders are the vital elements used in the VLSI designs. Adders are used in multiple blocks architecture of VLSI designs and Digital Computer Design. These are most frequently used digital components in digital integrated circuit design. Adders are important parameters for general purpose microprocessors and digital signal processing applications. Adders are not only necessary for addition, but it also needs for other parameter such as subtraction, multiplication and division. The performance adders are usually influence the fast and accurate operation of a digital system. Addition forms the basis for many processing operations, from ALUs to address generation to multiplication to filtering.. An extensive, almost endless, assortment of adder architectures serves different speed/power/area requirements.

II. Related Work

Mangesh B Kondalkar et al [1] proposed that fault tolerant adder implemented using kogge stone adder configuration can correct due to the inherent redundancy in the carry tree.

N.G.Nirmal and Dr. D.T.Ingole [2] proposed multiplier implementation with Kogge-Stone Adder as a basic component yields a significant reduction in Combinational path delay.

Vishnupriya.A and Sudarmani.R [3] proposed a new approach for high speed and low power multiplier design with less number of gate counts.. Kogge Stone adder (KSA) is used in place of counter for reducing the average connection delay.

Pakkiraiah Chakali and Madhu Kumar Patnala [4] proposed that Carry Select Adder (CSLA) is designed by using dual Ripple Carry Adders RCA and there is a scope for reducing delay in this.

V.Krishna Kumari and Y.Sri Chakrapani [5] proposed that Ripple Carry Adder (RCA) is serial adder and it has propagation delay problem. To overcome these issues we prefer parallel prefix adders such as KS adders, SKS adders, Spanning tree and Brent -Kung adders.

Ms. Madhu Thakur and Prof. Javed Ashaf [6] proposed that computational complexities of algorithms used in Digital Signal Processors (DSPs) have gradually increased.

III. Black Cell And Grey Cell

Kogge stone adder consists of mainly three components such as black cell, grey cell and buffer.

A. Black cell:

Black cells are used in the computation of both generate and propagate signals.

Pi (pres) = Pi and Pi (prev) (1)

Gi (pres) = (Pi and Gi (prev)) or Gi (2)

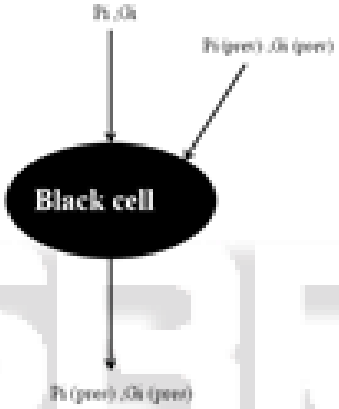


Fig. 1: Representation of Black Cell

B. Grey cell:

Grey cells are used in the computation of generate signals which are needed in the computation of sum in the post-processing stage.

Pi (pres) = Pi (3)

Gi (pres) =Gi (4)

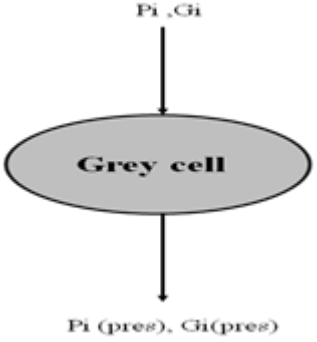


Fig. 2: Representation of Grey Cell

IV. Problem Description

Adders play an important role in filter design applications. Traditional adders delay increases as number of bits increases. It is required to design an efficient high speed adder to improve the performance of the filter.

V. PROPOSED SYSTEM

Kogge stone adder is a parallel prefix form of carry look ahead adder. Kogge stone adder can be represented as a parallel prefix adder graph consisting of carry operator nodes. The time required to generate carry signals in this prefix adder is 0(log n). It is the fastest adder with focus on design time and is the common choice for high performance adders in industry. The Kogge stone adder concept was devolved by Peter M. Kogge and Harold S. Stone which was published in 1973. In this adder generate and the propagate signals are precomputed. Usually in tree based adders, carriers are generated in tree and fast computation is obtained [3]. There are three stages in kogge-Stone adder they are

A. Pre Processing:

This step involves computation of generate and propagate signals corresponding too each pair of bits in A and B. These signals are given by the logic equations below:

Pi=Ai xor Bi (5)

Gi= Ai and Bi (6)

B. Carry look ahead network:

This block differentiates KSA from other adders. This step involves computation of carries corresponding to each bit. It uses group propagates and generate as intermediate signals which are given by the logic equations (7) and (8) respectively.

Pi:j = Pi:k+1 and Pk:j (7)

Gi:j = Gi:k+1 or (Pi:k+1 and Gk:j) (8)

C. Post processing:

This stage is common to all adders of this family (CLA). It involves computation of sum bits. Sum bits are computed by the logic given below:

Si = Pi xor Ci-1 (9)

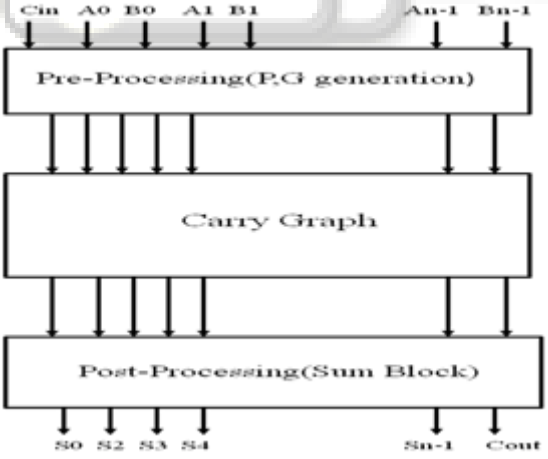


Fig. 3: Stages of Kogge Stone Adder

The parallel prefix Kogge- stone adder can be computed in many bits such as two-bit, three-bit, four-bit, seven-bit, eight-bit, sixteen- bit and thirty two-bit as well as. There are three inputs to the adder they are A (3:0), B (3:0) and Cin. The input Cin can be either '0' or '1'. These inputs are given to the respective propagate and generate blocks (PG) to produce propagate signal Pi (3:0) and generate signal Gi (3:0).These propagate and generate signal proceed to next stage. In this stage, it contains black cell, grey cell and buffer. The black cell executes both propagate and generate signal using equations (7) and (8).The grey cell executes only generate signal using equations (7). Finally the output Sum (3:0) is computed using equation (9) along with another output Cout

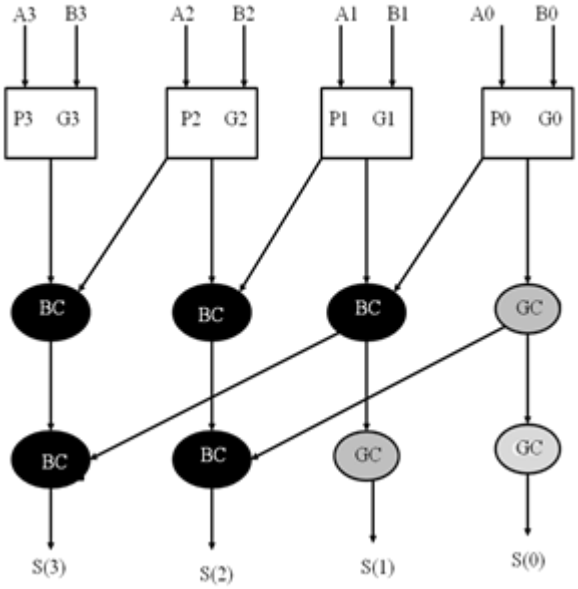


Fig.4: Four –bit Kogge stone adder

The eight-bit kogge stone adder is similarly implemented as that four-bit kogge stone adder as shown in Fig.5. There are three inputs to the adder they are A (7:0), B (7:0) and Cin. The input Cin can be either '0' or '1'. The output Sum (7:0) is computed along with another output Cout.

Consider an example to illustrate eight-bit Kogge stone adder A (8:0) =11111111, B (8:0) =11111111, Cin=0. The Sum output S (8:0) =1111111110, Cout=1.

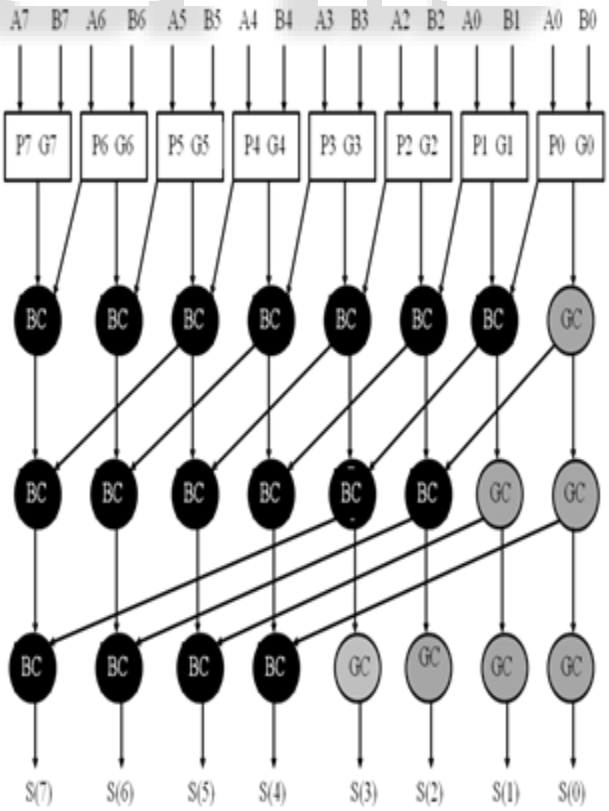


Fig. 5: Eight-Bit Kogge Stone Adder

D. Sixteen-bit kogge stone adder

The Parallel prefix sixteen -bit Kogge stone adder consists of a three inputs A (15:0), B (15:0) and Cin, Where the input Cin can either '0' or '1' .Outputs is Sum (15:0) and Cout. The Block diagram of sixteen bit Kogge stone adder is as shown in the Fig.6.

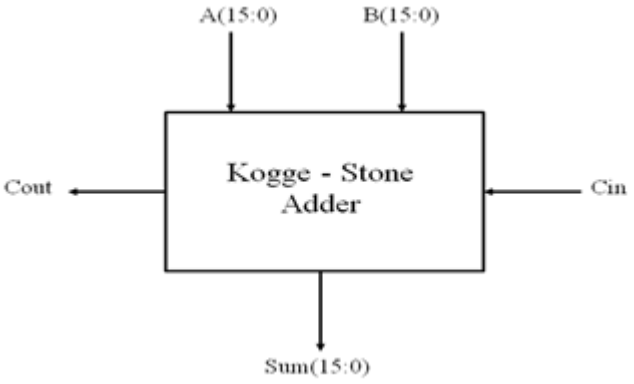


Fig. 6: Block diagram of Sixteen-bit kogge stone adder

It also consists of generate and Propagate Block (GP), Black cell (BC) and Grey cell (GC) similar to that four-bit Kogge-Stone adder.The representation of sixteen-bit Kogge-stone adder is as shown in Fig.7. Consider an example A (15:0) =1101101101101101, B (15:0) =1011011100101011, Cin=0. The Sum output S (15:0) = 1001001001011000, Cout=1.

Consider example A (15:0) =1111111111111111, B (15:0) =1111111111111111, Cin=0. The Sum output S (15:0) = 1111111111111110, Cout=1.

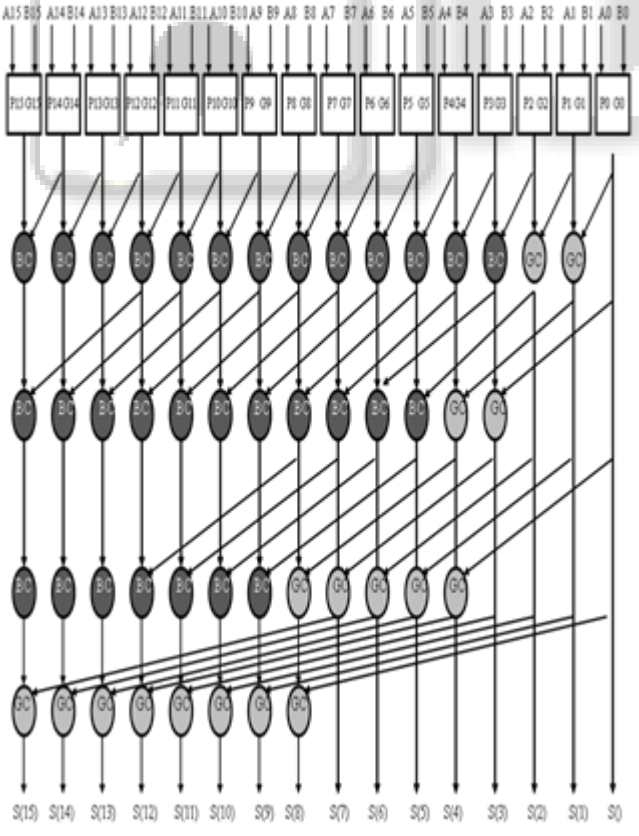


Fig. 7: Representation of Sixteen-Bit Kogge Stone Adder

VI. Application

The proposed sixteen-bit Kogge –Stone adder can be useful to convolute the discrete image samples with filter coefficients. The two discrete samples are multiplied and added. The filter coefficients are used to remove the noise in image by convoluting with image. Due to this the performance of speed can be improved. Convolution is a mathematical operation on two functions f and g, produce a third function that is naturally viewed as a modified version of one of the original functions, giving the area overlap between the two functions as a function of the amount that one of the original functions is translated.

$$(f * g)t = \int_{-\infty}^{\infty} f(\tau)g(t-\tau)d\tau \qquad (10)$$

Conversely, convolution can be derived as the inverse Fourier transform of the point wise product of two Fourier transforms. Computing the inverse of the convolution operation is known as De-Convolution.

Convolution filters are a great way to process images for certain features. Features are defined by an n*m matrix that is applied to the image. The Gaussian kernel of 3*3 is as shown in Fig.5.1.

VII. Result

The design proposed Parallel Prefix adder are coded in Verilog Hardware Description Language using structural modeling in Xilinx ISE Design Suite 14.5i and all the simulation results are verified using XILINX ISIM simulator. It is synthesized with Spartan-6 FPGA XC65LX45 with the speed grade of -2. Inputs are generated using Verilog HDL test bench.

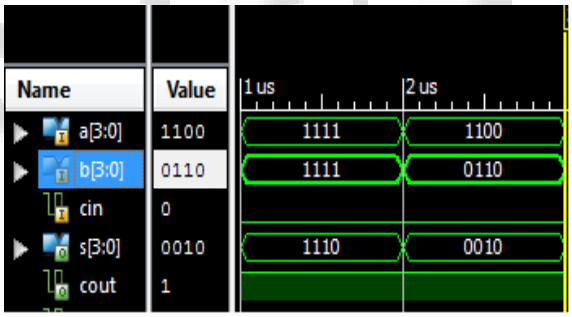


Fig. 6: Simulation Result of 4-Bit Kogge Stone Adder

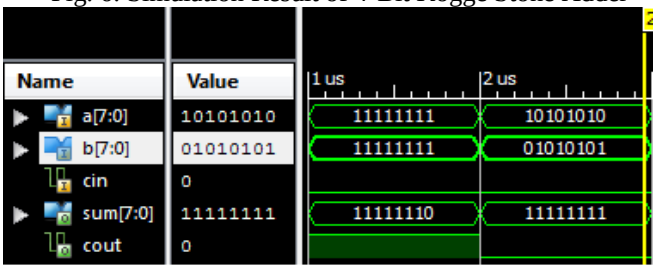


Fig. 7: Simulation Result of 8-Bit Kogge Stone Adder

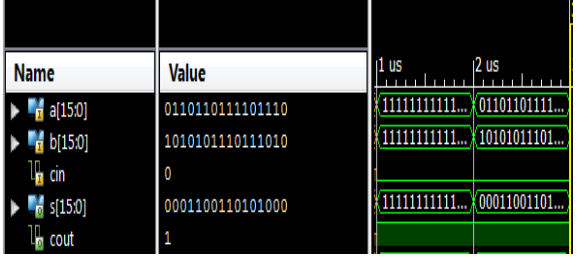


Fig. 8: Simulation Results of 16-Bit Kogge Stone Adder

VIII. PERFORMANCE ANALYSIS

The comparison is carried out in between the kogge stone adder and carry select adder with respect to the delay and area.

Table.1.Comparison of Delay and Area of kogge stone adder and carry select adder

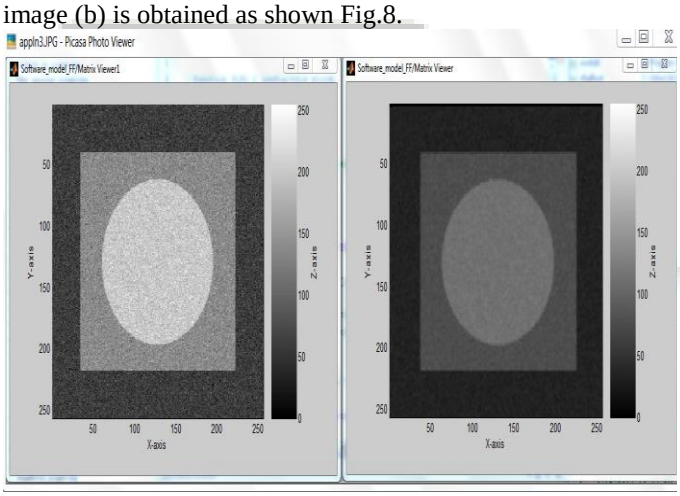
Parameter	**Carry select adder**		**Kogge stone adder**	
	4-bit	8-bit	4-bit	8-bit
Delay(ns)	11.91	17.682	10.618	16.191
No of LUT's	8	16	5	13

Table.2.Comparsion between 16-Bit Kogge Stone Adder and 16-Bit Brent-Kung Adder

PARAMETERS	**16-BIT KOGGE STONE ADDER**	**16-BIT BRENT KUNG ADDER**
Gate delay(ns)	21.303	20.589
No of slices	20	31
No of LUTS	37	55
No of IOs	51	51
No of bonded IOs	51	50

A. Convolution results

The results for convolution using sixteen-bit Kogge stone adder are shown. The results for input image (a) and output image (b) is obtained as shown Fig.8.



(A) INPUT IMAGE (B) OUTPUT IMAGE

Fig. 8: Mat lab results for convolution using proposed 16-bit kogge-stone adder

IX. CONCLUSION

In any digital or integrated systems, addition and multiplication are fundamental operations. Usually fast and accurate operation of digital system depends on performance of adders. Hence improving the speed by reduction in area is the main area of research in VLSI system design. Parallel prefix adders are type of adders, where execution is done in parallel. The comparison between kogge stone adders and carry select adder as done. The compared result shows that delay has been reduced in kogge stone adder compared to that of carry select adder. Here proposed Parallel Prefix architectures such as 16- bit Parallel Prefix Kogge Stone Adder is designed and implemented in Xilinx tool. The Comparison is done both on proposed adder in terms of delay and area. It is observed 16-bit Kogge stone adder as less delay compared to that 16- bit Brent-kung adder. The number of logic levels used is also found to be less. There is a reduction in both logic and routing delay and improvement in the speed. This proposed 16- bit Parallel Prefix Kogge Stone Adder is used in Convolution application. In this application the discrete image samples with filter coefficients

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