Low Power Pipelined RISC Processor: A Review

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Abstract— Reduced Instruction Set Computing or RISC is design strategy predicated on the CPU design strategy. Pipelining is the concept of overlapping of multiple Instructions during execution time. Pipeline is work on the task function it can splits one task into multiple subtasks. This paper is a fixated on pipelining concepts and the low power techniques which are required for the RISC CORE Processor .low power techniques avail to reduce power and heat dissipation and lengthen the battery life.

Keywords: RISC, Pipeline, low power

I. INTRODUCTION

Currently, On a single chip the computer architecture are implemented through the unprecedented IC fabrication technology Also, the current rate of process development allows implementations to be improved at a rate that is satisfying for most of the electronic tend in the markets these implementations serve. Microprocessors have grown from 8 bits to 16 bits, 32 bits, and currently to 64 bits. Microprocessor architecture has also grown from complex instruction set computing (CISC) based to reduced instruction set computing (RISC) based on a combination of RISC-CISC based and currently very long instruction word (VLIW) based execution are proceed. The most common RISC microprocessors are currently used in ARM, DEC Alpha, PA-RISC, SPARC, MIPS, and IBM's PowerPC. In the past five years there has been an explosive intensification in the instruction for portable computation and communication , The large processors working on the small portable phones, from portable telephones to sophisticated portable multimedia terminals . This interest in portable contrivances has fueled the development of low-power processors and algorithms, as well as the development of low-power general purpose processors. For the using of low power in RISC Processor it can reduce the heat dissipation and lengthen the battery life. In the Processor core area, the results of this attention to power are quite remarkable. This reduction has come as a product of fixating on the power dissipation at all levels of the design process, from algorithm design to the whole implementation. In the general purport processor area, however, there has been little work done to understand how to design energy efficient processors, which are used a less area and the speed is fast This is a commencement at bridging this gap and explores power and performance tradeoffs in the design and execution of energy- efficient , high speed RISC processors. Performance of processors has been growing at an exponential rate, doubling every 18 to 24 months, as the trade off the work in the field of power as is shown in The deplorable news is that the power dissipated by these processors has withal been growing exponentially Nowadays, computers are indispensable implements for most of the daily activities. With the fast change in the growing of the silicon technology and the decrementing cost of the integrated circuit, and a efficient RISC processor or central processing unit is incrementing widely utilized in every field of the technology . RISC is an extension of the architecture principles of the Reduced Instruction Set Computer (RISC). The simple design provides exceptional operation and is for apotheosis use in a broad family of cost-efficacious, compatible systems. Some typical applications include commercial data processing, computation-intensive scientific and engineering applications, and authentic-time control. Reduced instruction set computing, or RISC, is a Central processor design strategy predicated on the insight that simplified instruction can provide higher performance if this simplicity enables much more expeditious execution of each instruction . The trend in the recent past show the Reduce instruction set computing CPU clearly outsmarting the earlier CISC processor architectures. The reason have been the advantages, such as its easy, flexible and fixed instruction format and hardwired control system of logic , the load store quality it can access in the register so it is work on the register to register and which provide for higher clock speed so the performance is increased, by eliminating the necessacity for microprogramming. The combined advantages of high speed performance, low power, area efficient and performance -specific design hypothesis have make the RISC processor ubiquitous The advantages are, such as its simple, flexible and fine-tuned instruction format and hardwired control logic, which provide for higher clock speed, by eliminating the desideratum for microprogramming. This simplifies the instruction fetch mechanism since the location of instruction boundaries is not a function of the instruction type.

II. MAIN CHARACTERISTIC OF RISC PROCESSOR

The most common ways of overlapping are pre-fetching, pipelining and superscalar operation.

A) Pre-fetching:

The process of fetching next instruction or instruction into an event queue afore the current instruction is consummate is called pre-fetching. The earliest 16-bit microprocessor, the Intel 8086/8, pre-fetches into a non-board queue up to six bytes following the byte currently being executed thereby making them immediately available for decoding and execution, without latency.

B) Pipelining:.

Pipelining instruction betokens starting or issuing an instruction prior to the completion of the currently executing one. The current generation of machines carries this to a considerable extent. The PowerPC 601 has 20 separate pipeline stages in which sundry portions of sundry instruction are executing simultaneously.

C) Superscalar operation:

Superscalar operation refers to a processor that can issue more than one instruction simultaneously. The PPC 601 has independent integer, floating-point and branch units, each of which can be executing an instruction simultaneously.

CISC machine designers incorporated pre-fetching, pipelining and superscalar operation in their designs but with instruction that were long and involutes.

III. PIPELINING MECHANISM

In the RISC processor one instruction is execute when the next one is in decode process. It can increase the throughput of the system and is operand is loaded while the following instruction being fetched all at the same time .pipelining is a implementation technique where multiple instructions are overlapped. The non pipelined RISC architecture get more time to execute instruction compare to Pipelining architecture.

The fundamental principle behind pipelining is to sanction to commence the process of executing one instruction afore the antecedent one has consummated and it shows that even if there are delays in any one stage of the process for one instruction, it is still more efficient than non-pipelined processors. The latency is reduces through the pipelined architecture so speed is automatically increased. shows the processing of a sequence of instruction utilizing a rudimentary pipeline and shows the processing of a sequence of instruction utilizing 4-stage pipelined.

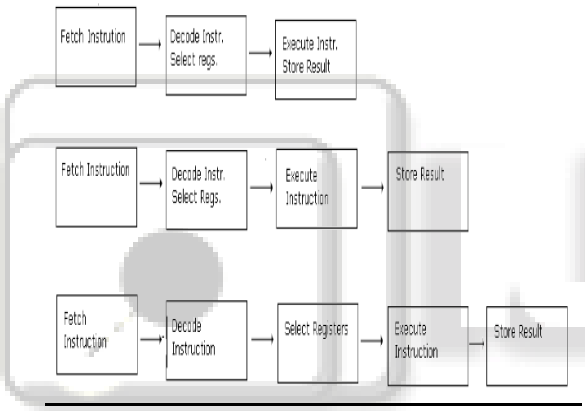

Fig.1: 3, 4, 5 stage pipelining

The four stages are-

Stage 1: Fetches instruction from memory.
Stage 2: Decodes instruction and fetches any required operands
Stage 3: Executes instructions
Stage 4: Stores results

- Fetch- Instruction memory- in the fetch number of instruction are drawn from instruction memory , in the instruction memory it contains the instruction that are executed by the processor.
- Program counter-The program counter contains the address of the instruction that will be fetched from the instruction memory during the next clock cycle. The pc is incremented by one during each given clock cycle.
- Decode- According to the control signal it can decode the instruction. which are come from fetch memory.
- Execute unit – The execution stage is where actual computation occurs. All the operations which are perform by the given control signals are executed..
- write back- In this stage, both single cycle and two cycle instructions write their results into the register file.

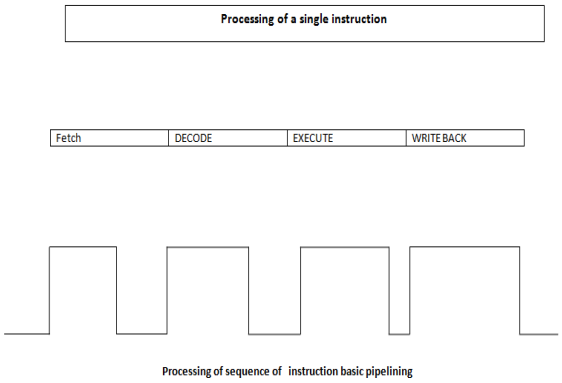

Fig. 2: Processing of sequence of instruction basic pipelining

A. Advantages of Instruction Pipeline

- The main advantages of instruction pipeline are:
- It's possible to utilize several control units for processing instruction but a single Pipelined control unit offers more advantages which can reduces power , increase speed factor
- Reduces requisite of hardware pipeline.
- Each stage performs only a portion of the pipeline stages and that no stage needs to incorporate a consummate hardware control unit.
- Each stage only needs the hardware associated with its existing task.
- The instruction -fetch stage only needs to read an instruction from memory. This stage does not require the hardware used to decode or execute instruction.
- Similarly a stage that decodes instruction does not access memory; the instruction fetch stage has already loaded the instruction from recollection into an instruction register for use at the decode stage.
- Another advantage instruction e pipelines is the reduced involution of the memory Interface. If each stage had a consummate control unit, ALL stages can access the memory and it can cause memory access conflicts in which the CPU must take care of.
- In general practice, RISC CPU has their recollection partitioned into instruction and data modules.
- The instruction-fetch stage reads data only from the instruction memory module at all other times; it is dealing with data in registers.
- The execute-instruction stage only access recollection when it is reading data from the Data recollection module. Custom designed recollection can be configured to sanction Simultaneous read/write access to different locations while evading recollection access Conflicts by the

execute-instruction and store-results stages of the pipeline

IV. TECHNIQUES FOR LOW POWER USED IN RISC PROCESSOR

As the portable ,battery operated ,electronics market move to computational intensive products like phone ,processor ,and note book computers need to focus on the power and extended the battery life of the system.

Dynamic Power Reduction-In the dynamic power reduction two technique mostly used-

- Cycle to cycle minimization- There are two more important approaches are used to reduction of a power in the resistor transfer level. the first approach is to minimize the power required to implement a function ,and second approach is to minimize the function needs to be executed. A new method of reducing the AC power was devised to minimize cycle to cycle unnecessary toggles .In the first method ,the upcoming next cycle can control signals and derived as a function of next cycle function, included the pervious cycle stage .so the toggle rate in the processor are minimize and power can be saved.

  This conception is simple one, if the functional path is not required a current cycle ,all the control path and data path are in the same state.
- Pseudo microcode- The microprocessor design a cull a decode method .In this method for every opcode , all control signal that can be set by that poodle are bundled together as a total identity .This includes the pipeline control ,and reduces the address generation control. In the pseudo microcode technique the decoder work as a rudimental of control signals when the control signal is given to any functional unit it is activate. and where there is no need of functional unit it can turn off the clock. According to the control signal is given to any functional unit it is activate ,and where there is no need of functional unit it can turn off the clock .according to the control signals it is activate .The power is reduced.
- Clock gating technique- The clock gating technique is required for the power consumption by flip flops and latches .so this technique is used for minimizing the power .The power is mainly consumed by combinational logics whose value are changing on the each clock edge ,flip flop .when the clock signal is not required particular block for some period it comes into an image and turn off the clock.
- Grey Technique- In the gray code is used for memory addressing schema instead of old binary coding .grey code addressing can significantly reduce the number of bit switching .The grey code addressing is a hardware method which uses for instruction address.

V. CONCLUSION

From the literature survey or review it is concluded that for the variants of application a particular type of RISC core with its different-2 configuration is Used . The work is done on the different stage of pipelining and fixate on the pipelining technique (3 ,4 ,5 stages) and how to reduce the power through power techniques utilized in the pipelined architecture from the pipelining stage is utilized it can increment the through put. And in this paper main objective is around in the power and other future work can done on speed and area.

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