AN EFFICIENT CONSTRUCTION OF ONLINE TESTABLE CIRCUITS USING REVERSIBLE LOGIC GATE

B. Sree Saranya¹

¹Department Of Computer Science And Engineering

¹ Saveetha School Of Engineering, Saveetha University Chennai, India

Abstract— Testable fault tolerant system style has become important for several safety vital applications. On the opposite hand, reversible logic is gaining interest within the recent late to its less heat dissipating characteristics. Any Boolean algebra perform is enforced mistreatment reversible gates. This paper proposes a way to convert any reversible gate to a testable gate that's additionally reversible. The resultant reversible testable gate will discover on-line any single bit errors that embrace Single Stuck Faults and Single Event Upsets S.Karp et al. The planned technique is illustrated mistreatment Associate in Nursing example that converts a reversible decoder circuit to an internet testable reversible decoder circuit.

Key words: Reversible gate, single stuck fault, testable gate

I. INTRODUCTION

Reversible Logic has gained importance within the recent past. The speedy decrease within the size of the chips has result in the exponential increase within the transit account per unit space. As a result, the energy dissipation is turning into a significant barrier within the evolving nanocomputing era. Reversible logic ensures low energy dissipation. Associate in Nursing operation is claimed to be physically reversible if there's no energy to heat conversion and no amendment in entropy. In reversible logic, the state of the machine device simply before Associate in Nursing operation is unambiguously determined by its state simply when the operation. In different words, no info concerning the machine state will ever be lost and thence the reversible logic are often viewed as a settled state machine. Computations performed by this computers unit normally irreversible, although the physical devices that execute them area unit essentially reversible. At the fundamental level, however, matter is ruled by Newtonian mechanics and quantum physics, that area unit reversible. With machine device technology chop-chop approaching the subatomic particle level, it's been argued again and again that this result gains in significance to the extent that economical operation of future computers needs them to be reversible. Hence, reversible logic is gaining grounds.

A reversible gate may be a logical cell that has constant range of inputs and outputs. Also, the input and output vectors have a matched mapping. Direct fan-outs from the reversible gate aren't permissible. Feedbacks from gate outputs to inputs aren't allowed. A reversible gate with n-inputs and n-outputs is named a n x n reversible gate. A previous analysis has been done on testable reversible circuits. Conditions for a whole take a look at set construction were mentioned and also the drawback of finding a minimum take a look at set was developed as Associate in Nursing whole number linear program with binary

II. DESIGN

A. Construction of on-line testable circuit:

This section describes associate degree algorithmic approach to convert any reversible circuit to a web testable reversible circuit. Given a reversible circuit consisting of reversible gates, the subsequent algorithmic rule converts it into a web testable reversible circuit.

Algorithm

Input: Reversible Circuit C
Output: a web testable reversible circuit CT

Construct C’ by substitution each reversible gate R in C by TRC(R). The parity input bits of TRC(R) area unit set specified herb = Pi within the construction of TRC(R).

By Lemma 2, C’ is reversible.

Fig. 1: Block diagram of TRC

(1) Let n be the number of reversible gates in C. Construct a (2n+1) x (2n+1) Test Cell (TC)
(2) First 2n inputs are the output parity bits from each of the n testable reversible cell TRC of C’ gate.
(3) The last bit of the input, called e, is either set to logic 0 or logic 1
(4) First 2n inputs are transferred to the output without any change

Fig. 2: Block diagram of TC

The technique planned during this paper are often utilized to convert any reversible circuit with capricious variety of gates to an internet testable reversible one and is freelance of the sort of reversible gate used. The made circuit will find any single bit errors that embrace single bit stuck-at-fault and single event upset S.Karp et al. A crucial advantage of the technique is that the logic style of a reversible circuit remains a similar and also the reversible circuit needn’t be redesigned for adding the testability feature thereto. Another advantage is that the technique ensures that the rubbish generated throughout the method of conversion to testable reversible circuit is reduced. The projected technique is illustrated victimization Associate in Nursing example that converts a decoder circuit that's designed by reversible gates to an internet testable reversible decoder circuit.
B. Constructable reversible circuit:

Theorem:
The cell TC made in formula has the subsequent properties:

1. It's reversible.
2. If there's one bit error in any TRC in CT, then T = one provided e = 0.
3. Perform T is enforced with minimum potential garbage.

Illustrated in Fig a pair of

Proof:
1. We can simply see that [Poa1, Pob1, . . . Poan, Pobn, 0] maps to [Poa1, Pob1, Poan, Pobn, T] and [Poa1, Pob1, . . . Poan, Pobn, 1] maps to [Poa1, Pob1, . . . Poan, Pobn, ?T], wherever T = [(Poa1? Poan) + (Poa2? Pob2). . . + (Poa? Pobn)] 7e?
   Therefore, TC is reversible.
2. Herb = Pib in TRC, from the step one of formula one. If there's one bit error in any TRC then by Lemma three, Poais complementary to letter box. Therefore, Poa? letter box = one. Therefore T = one.
3. For AN n-input k-output perform f, the minimum range of garbage bits needed to create it reversible is ceil(log M), wherever M is that the most range of times AN output pattern is recurrent D.Maslov (2004). For the perform T, M = 22n – 2n
   Where n is that the range of TRCs in CT.
   Therefore, log M = log (22n– 2n) &gt; (2n - 1). Therefore, ceil (log M) = 2n.
   The rubbishes that square measure generated for any circuit that's enforced victimization the cascaded block of R1 and R2 in D.P.Vasudevan et.al (2004), are going to be definitely larger than or adequate to the circuit enforced victimization TRC(R). As an example a 2 input AND gate enforced victimization R1 gate generates additional a pair of garbage bits compared to TRC (Toffoli gate), the two combine rail checker employed in D.P.Vasudevan et.al (2004) to notice errors is built from six R3 gates and produces garbage of eight bits. For a reversible circuit with 2n testable reversible gates the technique planned in D.P.Vasudevan et.al (2004) generates garbage of 8n bits wherever because the take a look at Cell, TC, generates garbage of 2n bits. This paper proposes a hierarchal construction for on-line testable reversible circuits. Contemplate a reversible circuit C that's the combination of the individual reversible modules Ci ∀i = one, 2, . . . k. Ci is created on-line testable by applying formula.
   A Multi standard Testable Cell MMTC is employed to notice errors within the microcircuit C.

MMTC is defined as follows:

Inputs: T1, T2, . . . .Tn and e, wherever e will be either zero or one.
Inputs: T1, T2, . . . .Tn and e, wherever e will be either zero or one.
Outputs: T1, T2, . . . .Tn and MMT = (T1 + T2 + . . . + Tn) ⊕ e.

Theorem: The cell MMTC has the subsequent properties:

1. It's reversible.
2. MMTC detects any single bit error in C1, C2, . . . . Ck, wherever Ci may be a on-line testable reversible module Vi.
3. Perform MMTC is enforced with minimum attainable garbage.

Proof:
1. We will simply see that [T1, T2, . . . Tn, 0] maps to [T1, T2, . . . Tn, MMT] and [T1, T2, . . . Tn, 1] maps to [T1, T2, . . . Tn, ¬MMT] and MMT = (T1 + T2 + T3 + . . . + Tn) ⊕ e thus, MMTC is reversible.
2. Ti bit is that the take a look at bit from the TC of module Ci. The multi detected.
3. The minimum variety of garbage bits needed to create perform MMTC reversible is ceil(log M), wherever M is that the most variety of times AN output pattern is continual within the truth table of MMTC, D.Maslov et.al (2004). For the perform MMTC, M = 22k - one, wherever k is that the variety of on-line testable reversible modules. Therefore, ceil (log M) = log (22k - 1) = 2k therefore, the.

III. ILLUSTRATIONOF THE PROJECTED TECHNIQUE

To illustrate the projected technique, a reversible decoder circuit is born-again to an internet testable reversible decoder. A decoder may be a combinative circuit that converts binary info from n input lines to a most of 2n distinctive output lines. Allow us to think about a 2-to-4 decoder with the alter bit. The development of the reversible decoder circuit uses 3 Fredkin gates, A and B area unit the one-bit inputs to the decoder; E is that the one-bit alter and O1, O2, O3 and O4 area unit the output bits of the decoder. Rule is applied to convert the decoder circuit into an internet testable one. we have a tendency to illustrate this system in a very elaborate step by step manner.

Input: Reversible Decoder Circuit C
Step one: Replace Fredkin gate Fk with its Testable Reversible TRC (Fk) for k = 1, 2, 3. Let the input vector of Fk be [a, b, c] and also the output vector be shown in figure Fig three.

Decoder Truth Table
Step one: Replace Fredkin gate Fk with its Testable Reversible TRC (Fk) for k = 1, 2, 3. Let the input vector of Fk be [a, b, c] and also the output vector be [O1, O2, O3, O4]. The deduced Fredkin gate, DRa is obtained like the subsequent because the inputs and outputs:

Inputs: a, b, c and Pia
Outputs: O1 = a; O2 = a ⊕ ab ⊕ ac
O3 = b ⊕ ab ⊕ ac; Poa = O1 ⊕ O2 ⊕ O3 ⊕ Indian arrowroot
Poa = (a) ⊕ (c ⊕ ab ⊕ ac) ⊕ (b ⊕ ab ⊕ ac) ⊕ (Pia) = a ⊕ b ⊕ c (Pia)

The truth table of the deduced Fredkin gate DRa is shown. To construct DRb, take X to be a three x three gate that has inputs as [I1, I2, I3] and outputs as [U1, U2, U3], wherever Ui and Ii are unit connected as Ui = li for i = one, 2, 3.

The deduced gate DRb is as shown in Figure eleven, with the subsequent because the inputs and outputs:

Inputs: I1, I2, I3 and Pib
Outputs: U1 = li wherever i = one, 2, 3.
Pob = Pib ⊕ U1 ⊕ U2 ⊕ U3 = Pib ⊕ I1 ⊕ I2 ⊕ I3

Truth table of DRb is as shown in Table III. we have a tendency to cascade the higher than 2 deduced gates, DRa and DRb to induce a Testable Reversible Fredkin Cell (TRC). Pia = Pib, allow us to set them to logic zero. This completes the development of TRC(R) for the Fredkin gate. currently we have a tendency to replace every Fredkin gate Fk for k = one, a pair of and three within the input decoder circuit with TRC(R) created higher than.

Step 2: Add a take a look at Cell (TC) with 2n + one input line. As n = three for the given decoder circuit, TC has 2n+1 = seven input lines. Connect its initial six input lines to the parity bits Poak and Pobk of the Fredkin gates Fk for k = one, two and three as shown in Figure twelve. initial six input lines area unit passed to the output lines with none amendment. Output bit T is that the error police work bit. the worth of T can confirm if there's a mistake within the circuit.

Output: Circuit therefore obtained is shown in Figure twelve and is that the needed on-line testable reversible decoder circuit CT. allow us to take into account the case once the input vectors [A, B, E] = [1, 0, 1]. From the reality Table I, if the circuit is error free, output vector O ought to be [0010]. during this case, the parity vector [Poa1, Pob1, Poa2, Pob2, Poa3, and Pob3] is capable [0, 0, 1, 1, zero and zero] and T = 0 that shows that the circuit is error free.

Fig. 3: Truth table for DRG
during this case, the parity vector [Poa1, Pob1, Poa2, Pob2, Poa3, and Pob3] is adequate to [0, 0, 1, 1, zero and zero] and T = 0 that shows that the circuit is error free. Suppose there's some error within the circuit, say in F1. For the given input vector [A, B, E] = [1, 0, 1], output of F1 is [1, 1, 1] rather than [1, 0, 1]. In this case, parity vector [Pia1, Pib1, Pia2, Pib2, Pia3, Pib3] it's clear-cut to infer that if there's any single bit error within the circuit, it'll be indicated by the error bit T. If the reversible circuit is created of over one modules, then mistreatment the hierarchical data structure these is integrated by mistreatment MMTC creating it on-line testable. Figure five shows the diagram of of on-line testing 2:4 decoder.

Fig. 4: Block diagram of online testing 2:4 decoder
Test cell output

Fig. 5: Decoder with online testing with TC
Multimodular test cell output

Fig. 7: Decoder with online testing with MMTC

IV. CONCLUSION
In this paper, we have a tendency to planned a strategy that converts any reversible gate into a testable reversible gate, mistreatment an equivalent, any reversible circuit manufactured from reversible gates may be regenerate to an internet testable one with minimum garbage. The resultant testable circuit will discover on-line any single bit errors that embrace Single Stuck Faults and Single Event Upsets. a vital advantage of the technique is that the planning of a reversible circuit needn't be modified for the aim of adding testability feature thereto. This paper proposes the development of multi-modular on-line testable reversible circuits hierarchically.

REFERENCES


