Comparative Study of LDPC and Viterbi Decoder

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Abstract— The main concern in any communication system is the reliable transmission of signals of information from a transmitter to a receiver. The signals are transmitted via a channel which corrupts the signal. It is necessary that the distorting effects of channel and noise are minimized and that the information sent through the channel in any given time is maximized. Channel coding techniques are employed to do this. In this paper we discuss the different decoders used to decode the channel encoded data.VLSI implementation complexity of a low density parity check (LDPC) decoder is heavily affected by the inter-connect and the storage requirements.. Several structured properties of LDPC codes and decoding algorithms are observed and are used to construct hardware implementation with reduced processing complexity. Another technique, known as Convolutional encoding is used for correction of errors at the receiver end .Convolutional codes protects information by adding redundant bits to the binary data. Viterbi decoding is the technique for decoding the Convolutional codes. The Viterbi algorithm estimates the maximum likelihood path through a trellis based on received symbols.

I. Introduction

A. *Ldpc decoders*

Low-density parity-check (LDPC) codes are a class of linear block LDPC codes. The name comes from the characteristic of their parity-check matrix which contains only a few 1's in comparison to the amount of 0's. Their main advantage is that they provide a performance which is very close to the capacity for a lot of different channels and linear time complex algorithms for decoding [1]. Furthermore are they suited for implementations that make heavy use of parallelism. They were first introduced by Gallager in his PhD thesis in 1960. Gallager, But due to the computational effort in implementing coder and en- 1960 coder for such codes and the introduction of Reed-Solomon codes, they were mostly ignored until about ten years ago. LDPC decoding uses a layered offset-min-sum algorithm , so most central FUs are used differently than for turbo decoding. A big difference is the interconnect operation. The 4x4 crossbar is coupled with a barrel shifter stage to provide.

B. *Viterbi decoder:*

Viterbi decoders work on Viterbi algorithm to decode the encoded data. The Viterbi decoding algorithm was discovered and analysed by Viterbi in 1967. The Viterbi algorithm essentially performs maximum likelihood decoding; however, it reduces the computational load by taking advantage of the special structure in the code trellis. The algorithm involves calculating a measure of similarity, or distance between the received signal, at time t_i, and all the trellis paths entering each state at time t_i. The Viterbi algorithm removes from consideration those trellis paths that could not possibly be candidates for the maximum likelihood choice. When two paths enter the same state, the one having the best metric is chosen; this path is called the surviving path. This selection of surviving paths is performed for all the states. The decoder continues in this way to advance deeper into the trellis, making decisions by eliminating the least likely paths. The early rejection of the unlikely paths reduces the decoding complexity. In 1969, Omura demonstrated that the Viterbi algorithm is, in fact, maximum likelihood. Note that the goal of selecting the optimum path can be expressed, equivalently, as choosing the codeword with the maximum likelihood metric or as choosing the code word with the minimum distance metric[2&3].

II. Architecture

A. *LDPC's architecture:*

The circular matrix permutations that are required for aligning the message vectors associated with the sub matrices of a parity-check matrix to the PEs. The Gamma FU is used to subtract extrinsic value from the current bit value. In the Alpha-beta FU the minima search and LLR accumulation operations of the min-sum algorithm are performed. The new extrinsic value is recombined with the bit value in the DALU FU. LMEM is again used as intermediate storage [4].

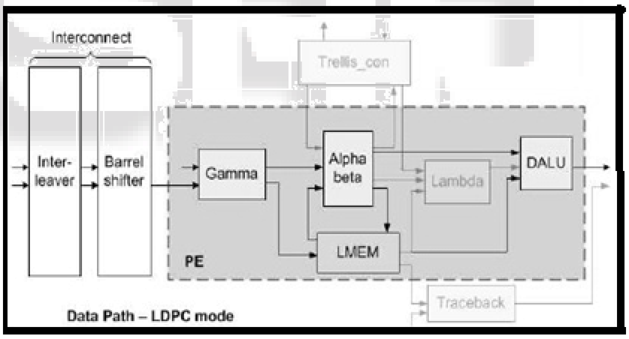

Fig. 1: Data path –LDPC mode

B. *Viterbi's Architecture*

Generally, a Viterbi decoder consists of three basic computation units: Branch Metric Unit (BMU), Add-Compare-Select Unit (ACSU) and Trace Back Unit (TBU).

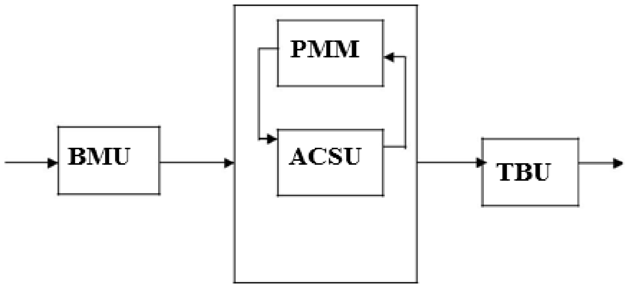

Fig. 2: Block diagram of Viterbi decoder

1) Branch metric unit (BMU)

The branch metric unit calculates the branch metrics by the hamming distance or Euclidean distance. The branch metric computation block compares the received code symbol with the expected code symbol and counts the number of differing bits. The Branch Metric Unit is designed using the EXOR gate and the 3-bit counter [5].

2) Add-Compare Select unit (ACSU)

The Add-Compare Select Unit (ACSU) adds the Branch Metrics (BM) to the partial Path Metrics (PM) to obtain new path metric. When two paths enter the same state, it compares the new PMs and the one having minimum metric is chosen , this path is called survivor path. The selection for survivor path is done for all states. It then stores the selected PMs in the Path Metric Memory (PMM). The PM of the survivor path of each state is updated and stored back into the PMM.

3) Trace Back Unit (TBU)

The final unit is the trace-back process or register exchange method, where the survivor path and the output data are identified. The trace-back (TB) and the register-exchange (RE) methods are the two major techniques used for decoding the output sequence. The TB method extracts the decoded bits; beginning from the state with the minimum PM. Beginning at this state and tracing backward in time by following the survivor path, which originally contributed to the current PM, a unique path is identified. While tracing back through the trellis, the decoded output sequence, corresponding to the traced branches, is generated in the reverse order.

III. RESULT AND COMPARISON

	Single-mode	Multi-mode	Increase (%)
Viterbi	11.5 mW	24.9 mW	116
Turbo	26.6 mW	31.6 mW	19
LDPC	23.3 mW	33.4 mW	14

Table3: Estimated power consumption (without memories)

We have shown the implementation of three decoder cores for convolutional, turbo and LDPC codes, respectively, that are all derived architecturally from one multi-mode ”mother” decoder capable of decoding all three code types. In comparing the implementation results for these decoders, we were able to show that combining Viterbi and turbo decoding incurs an area overhead of roughly 10% over just the turbo decoder[6]. Taking only the data paths into account, the combined Viterbi/turbo/LDPC decoder has an area advantage of about 26% compared to the sum of all three decoders. There is however a heavy penalty on the power consumption of the multi-mode decoder, which leads to the conclusion that it only makes sense to employ a multi-mode solution in an environment that is not completely focused on low-power. An obvious example would be a base station in mobile communications[7].

IV. APPLICATION OF VITERBI DECODER

A. LDPC:

(1) G.hn/G.9960 (ITU-T Standard for networking over power lines, phone lines and coaxial cable)
(2) 802.3an (10 Giga-bit/s Ethernet over Twisted pair)
(3) CMMB(China Multimedia Mobile Broadcasting)
(4) DVB-S2 / DVB-T2 / DVB-C2 (Digital video broadcasting, 2nd Generation)
(5) DMB-T/H (Digital video broadcasting).
(6) WiMAX (IEEE 802.16e standard for microwave communications)
(7) IEEE 802.11n-2009 (Wi-Fi standard)[8].

B. VITERBI:

(1) Radio communication: digital TV ATSC, QAM, DVB-T, etc.), radio relay, satellite communications, PSK31 digital mode for amateur radio.
(2) Decoding trellis-coded modulation (TCM), the technique used in telephone-line modems to squeeze high spectral efficiency out of 3 kHz-bandwidth analog telephone lines.
(3) Computer storage devices such as hard disk drives.
(4) Ultra wide band application.
(5) Voice band data application.
(6) Automatic speech recognition [9].

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