A Review on Clock Gating Technique for Power Reduction in VLSI Designs

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Abstract--- Pulsed-latched circuits, in which latches are triggered. In today’s world, with increasing complexity of the chip, the transistor count reached over millions of transistor. Also demand for high speed performance tends to increase the clocking frequency. With the increase in clock frequency, also the switching activity in the synchronous digital design has increased largely, increasing the dynamic power dissipation due to switching. Hence it has become necessary to reduce the power losses in due to switching activity. For such reduction clock gating technique is applied, in which the clock signal is disabled during the period of inactivity. In this paper a review of present clock gating techniques is done.

Keywords: - clock gating, low power design, sequential circuit,

I. INTRODUCTION

In a system, the sequential circuits are the major contributors of the power dissipation since one of the inputs of sequential circuits is the clock signal, which is the signal that switches all the time. Also the state of art designs with enhanced speed operate at high frequency as it has to drive more load to reach to many sequential elements in the chip. Hence due to frequency clock signals are the greatest source of dynamic power dissipation. Clock signal do not carry any information and does not do any computation. They are mainly used for synchronization. Also recent study shows that the clock signals in digital computers consume a large percentage (nearly 15–45%) of the system power [1]. Thus, the system power loss can greatly be reduced by reducing the clock power dissipation. So in order to reduce the dynamic power loss, gate clocking technique is used.

In clock gating, the clock of the sequential block of the device is shut off if no operation is required from that section of the circuit for some duration of time. In the synchronous digital circuits the clock net responsible for significant part of power dissipation i.e., up to 40% [4]. By applying clock gating the unwanted switching of the clock net can be reduced by disabling the clock. Clock signal continuously consumes power as it toggles the registers and their associated logic. More power can be saved by not toggling the register if it does not change its state. So clock gating shuts off the clock while the system maintains its current state. In this paper a review of present clock gating techniques is made. Present there are many clock gating techniques available, from which, in this paper basic clock gating techniques are discussed.

II. BASIC TECHNIQUES FOR CLOCK GATING

Initially, many authors suggested the basic techniques of clock gating using AND gates, NOR gates, AND latch and NOR latches. In this paper, first these techniques will be discussed.

A. AND gate

Because of the simple logic of AND gate, a 2 input And gate is inserted in sequential logic for gating the clock [3]. One of the input to the AND gate is clocked while in the second input a signal which is used to control the output of the sequential circuit is given as shown in Fig. 1. This enable signal will at last control the clock to the sequential circuit.

![Fig. 1: AND based clock gating](image)

B. NOR gate

NOR gate is a very suitable technique for clock gating where actions are needed to be performed on Positive edge of the global clock. [4]. One of the input to the NOR gate is clocked while in the second input a signal which is used to control the output of the sequential circuit is given as shown in Fig. 2. This enable signal will give inverted as it’s a NOR gate.

![Fig. 2: NOR based Clock Gating](image)

For avoidance of glitches to appear, and gate clock gating technique should be used positive edge triggered system. The output in this case could be wrong. Also the problem of hazards could occur when any hazard at the EN could be pass on to the GATED_CLK when CLK=’0’. This system is very dangerous and could jeopardize the correct functioning of the entire system [31].

C. Latch based AND gate clock gating
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D. Latch based NOR gate clock gating

III. CLOCK GATING

Clock gating is an effective way of reducing the dynamic power dissipation in digital circuits. In a typical synchronous circuit such as the general purpose microprocessor, only a portion of the circuit is active at any given time. Hence, by shutting down the idle portion of the circuit, the unnecessary power consumption can be prevented. One of the ways to achieve this is by masking the clock that goes to the idle portion of the circuit.

Clock-gating is a well-known technique to reduce clock power. Because individual circuit usage varies within and across applications, not all the circuits are used all the time, giving rise to power reduction opportunity. By ANDing the clock with a gate-control signal, clock-gating essentially disables the clock to a circuit whenever the circuit is not used, avoiding power dissipation due to unnecessary charging and discharging of the unused circuits. Specifically, clock-gating targets the clock power consumed in pipeline latches and dynamic-CMOS-logic circuits (e.g., integer units, floating-point units, and word-line decoders of caches) used for speed and area advantages over static logic.

Effective clock-gating, however, requires a methodology that determines which circuits are gated, when, and for how long. Clock-gating schemes that either result in frequent toggling of the clock-gated circuit between enabled and disabled states, or apply clock-gating to such small blocks that the clock-gating control circuitry is almost as large as the blocks themselves, incur large overhead. This overhead may result in power dissipation to be higher than that without clock-gating.

IV. CLOCK GATING

A. Simple 4 Bit Counter without Clock Gating

A simple 4 bit up counter is simulated first without applying clock gating. Its RTL view is shown in fig 8.
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B. Simple 4 Bit Counter With and Gate Clock Gating

AND gate clock gating is applied to the counter by inserting a simple AND gate as shown in fig. 4.5 gated 4 bit counter. From Fig 4.5 it can be seen that a simple two input AND gate is placed before the counter to clock gate the clock signal.

C. Simple 4 Bit Counter With nor Gate Clock Gating

NOR gate clock gating is applied to the counter by inserting a simple NOR gate as shown in fig. 14. From Fig 14, it can be seen that a simple two did not input NOR gate is placed before the counter to clock gate the clock signal. However, the enable signal to the NOR gate is given through an inverter with respect to the behavioural function of the NOR gate.

In fig 15, a detailed RTL Technology of the 4 bit counter is shown. Fig.16 shows that by using an NOR gate clock gating technique with counter there is reduction in switching activity of the counter. The counter increases only when enable signal is asserted low and clock event occur. This results in reduction of the switching activity of the counter and hence reduction in the dynamic power consumption of the counter occurs.

Fig. 10: Simulation waveform of counter

Fig. 11: RTL Schematic of AND

In fig 4.6, a detailed RTL Technology of the 4 bit counter is shown.

Fig. 12: RTL Technology of AND gated 4 bit counter.

Fig. 13: Simulated waveform of AND gated counter

Fig. 14: RTL Schematic of NOR gated 4 bit counter

Fig. 15: RTL Technology of NOR gated 4 bit counter

Fig. 16: Simulated waveform of NOR gated counter

Fig. 17: Simulation Summary
V. CONCLUSION

Clock gating is the technique, used to selectively stop the clock of the sequential elements to reduce unnecessary switching activity. Hence reduce the power consumption.

The AND gate based and NOR gate based clock gating techniques are applied to a simple four bit counter. The total power consumption of counter without clock gating is 35.81 mW. While the total power consumption of counter with AND gate based clock gating is total power consumption. However negative results is obtained for NOR gate based clock gating. Its total power consumption is 36.45mW, which is more than counter without clock gating.

REFERENCES