Voltage Level Shifters – Review

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Abstract— A review on various CMOS voltage level shifters is presented in this paper. A voltage level-shifter shifts the level of input voltage to desired output voltage. Voltage Level Shifter circuits are compared with respect to output voltage level, power consumption and delay. Systems often require voltage level translation devices to allow interfacing between integrated circuit devices built from different voltage technologies. The choice of the proper voltage level translation device depends on many factors and will affect the performance and efficiency of the circuit application.

I. INTRODUCTION

In CMOS circuits, the dynamic energy is directly proportional to supply voltage. As the supply voltage is higher, the energy consumption is more. Thus, to reduce dynamic energy consumption we use low supply voltage in a circuit, without affecting its suitability for the desired purpose. However, when a high voltage circuit is driven by a low voltage circuit, the PMOS of the high voltage gate may not turn off completely by the low voltage "high logic" input. The requirement of voltage level shifter arises here. When low voltage gates need to drive high voltage gates, the level-up shifters are used.

The more number of circuits can be designed on a single chip called System on Chip (Soc) in which the entire system can be fabricated on a single chip. However, the major concern is related to the fact that different gates can use different voltage levels. The output from a high voltage gate can be connected to the input of a low voltage gate and vice versa. Another purpose to use the level shifter circuits is the different voltage requirement between the voltage levels of core circuits and I/O circuits in multi-voltage devices. In multi-voltage level devices multiple blocks work on different voltages. Therefore, when signal passes from one block to another block, level shifters are necessary. The integrated circuits will have high packaging density and reduced power consumption if we scale down the size of transistors used. However, major devices still use the 3.3V technology so level shifter circuits can play an important role in digital circuit designs.

However, there are few disadvantages with level shifter. The level shifter increases the total area of the circuit, due to which, the power dissipation increases. The level shifter circuit becomes more complex and error prone as the difference between the two voltage levels increases. Therefore, it is desirable for the level shifter design to be attractive in reducing power consumption, delay and area while maintaining its intended purpose. [1].

An alternative approach, known as the multi-supply voltage domain technique, consists of partitioning the design into separate voltage domains (or voltage islands), each operating at a proper power supply voltage level depending on its timing requirements. Time-critical domains run at higher power supply voltage (VDDH) to maximize the performance, whereas noncritical sections work at lower power supply voltage (VDDL) to improve power efficiency. For extremely low-power applications, the presence of sections of the system operating in a sub-threshold regime is a valuable option [2].

This paper is illustrating various architectures of voltage level shifter circuits employed in different application. The different parameters related to voltage level shifter circuit are also summarized in this survey.

II. VOLTAGE LEVEL SHIFTER 1

This section includes different architectures of conventional voltage level shifter and their functioning. The conventional level-shifter circuit using cross-coupled PMOS load is shown in Fig. 1 [1]. This conventional level shifter for high-voltage drivers usually applies High Voltage NMOS (HVNMOS) and High Voltage PMOS (HVPMOS) as the pull-up and pull-down devices. This conventional level shifter translates voltage from a low voltage supply (VDDL) to high voltage supply (VDDH). The pull-down NMOS has to overcome the PMOS latch action before the output changes state. When input is low, MN1 and MP2 are turn-on and MN2 and MPI are turn-off and out node is VDDH. If input switches to high, MN2 and MP1 are turn on and MNM and MP2 is turn-off and Vout is low. Therefore, the output voltage experiences full swing from 0 to VDDH.

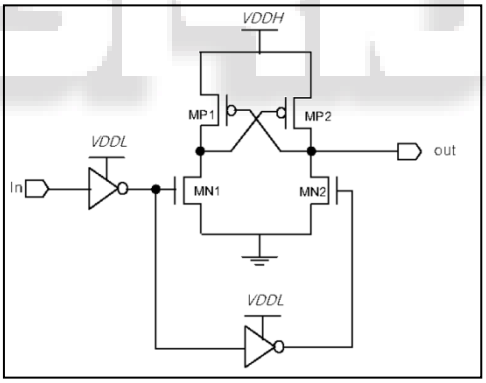

Fig.1: Conventional voltage level shifter circuit 1

This conventional level-shifter, on the other hand, has Some critical problems in high voltage circuits such as display panel drivers. The full-swing output of level-shifter damages the gate oxide of transistors. The Vgs of MP1 and MP2 in level-shifter as well as pull-up PMOS and pull-down NMOS of output drivers experience full voltage swing from 0 to VDDH. [2] Usually, the drain to source breakdown voltage (Vds) is very high for HV (High Voltage) devices while the gate to source breakdown voltage (Vgs) is much lower. For a 0.35um process, the Vgs breakdown voltage of HVNMOS is about 5V and the Vds breakdown voltage is higher than 20V. [4]

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III. VOLTAGE LEVEL SHIFTER 2

Separated and low swing output level-shifter is shown in Fig. 2. In Fig. 2, two bias voltages are used to limit the voltage swing of the output node out hl, out 11. When the input is high, M2 turns on and pulls down the out 11 node to GND. The generated large Vgs of M4 will turn on the M4 and pull the node MND1 to GND. M6 and Bias h will keep Out hl lower than Bias h+|Vthp| (If Out_hl is higher than Bias h+|Vthp| , M6 will turn-on and pull the node out_hl down to Bias_h+|Vthp|. The cross-coupled transistor M7 and M8 operate like a current sense circuit. It will further pull down the voltage of out_hl node to about Bias-h. On the contrary, when the input is low, the Out_hl output will be high and the Out 11 will be low. It can prevent Vgs breakdown of level-shifter and output driver's pull-up and pull-down transistors.

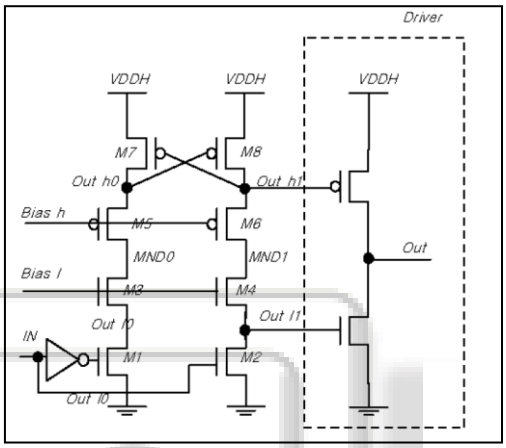

Fig.2: Conventional voltage level shifter circuit 2 [4]

In this circuit, the number of Bias (Bias_h, Bias_l) depends on the VDDH and Vgs breakdown voltage of transistors. If VDDH is more high and Vgs breakdown voltage is low, more bias levels are required, and in the case of VDDH variation. Level-shifter's output swing level (VDDH, VDDH-Bias_h-|Vthp|) depends on the VDDH.

IV. VOLTAGE LEVEL SHIFTER 3

This circuit adopts a conventional cross-coupled level-shifter configuration (Fig. 3). M2 and M3 are used as pull-ups to drive V_{DN6} and V_{DN7} to VPP, and to ensure the output EDPMOS is turned completely off or on. To prevent exceeding V_{BOX} when either M6 (VIN high) or M7 (VIN low) are on, and when the HV supply exceeds 30V, M1 and M4 are used to limit the voltage drop across V_{DN6} or V_{DN7} to $V_{PP} - VDD$.

The major drawback of this design is the continuous power dissipation in both output high and output low due to the fully on pseudo-NMOS (LDMOS pull-down and PMOS2 pull-up) configuration.

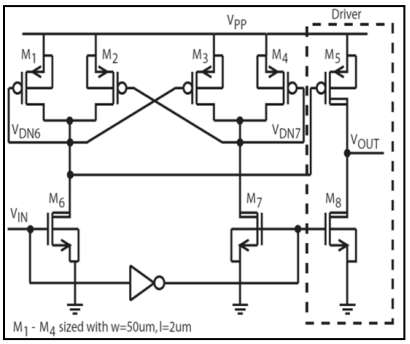

Fig.3: Pseudo NMOS voltage level shifter circuit 3 [5]

From simulation results in Fig. 4, a constant 2.69mA of current flows through the drain terminal of M6 or M7 in either case, which at VPP = 300V results in over 800mW of quiescent power.

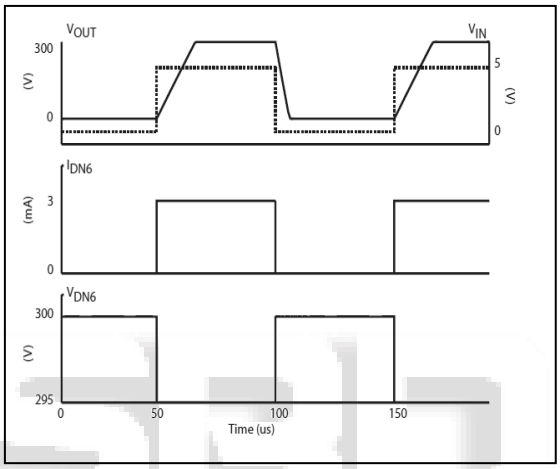

Fig.4: Simulation results of circuit 3

V. VOLTAGE LEVEL SHIFTER 4

In this circuit power consumption is reduced through dynamic control of the charge on the gate of the output EDPMOS transistor. Fig. 5and 6 show the circuit and corresponding simulations.

A strobe signal, VIN1, controls the operation of the level shifter. When M2 is off and the strobe signal is high, C1 is discharged and the output EDPMOS is turned off. However, if M2 and the strobe are high at the same time, M2 carries a 750μA drain current, causing a 5V drop across the PMOS2 load transistor M5. When the strobe and VIN2 signal go low, V_{GP6} is isolated and the voltage drop is ideally retained. However, because of sub threshold leakage through M5 (and other sources of leakage), VGP6 must be periodically refreshed to maintain the level-shift operation.

Because the majority of power consumption occurs during the strobe pulses, low average power dissipation is achieved by ensuring the duration of the strobe pulse is small (i.e. 200 ns). Also, because of already available dynamic control of input signals, crowbar current at the output stage can be eliminated by ensuring M3 is off before the EDPMOS turns on for output high, and turning the EDPMOS on only after the output stage LDMOS has been turned off for output low. Though not demonstrated here, crowbar current can also be eliminated in the static circuits.

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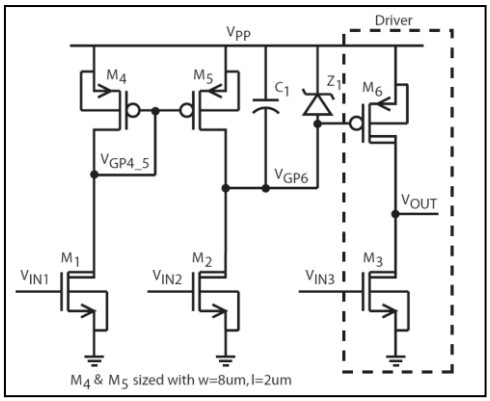

Fig.5:Dynamic voltage level shifter circuit 4 [5]

To reduce power dissipation further, an improved design takes advantage of the Zener diode, Z1. With Z1 designed for a breakdown voltage of less than 15V (to prevent V_{BDS} of the PMOS2 M5), M2 now only needs to be pulsed for output high (rather than also pulsing the strobe signal), thus eliminating the additional current draw through M1.

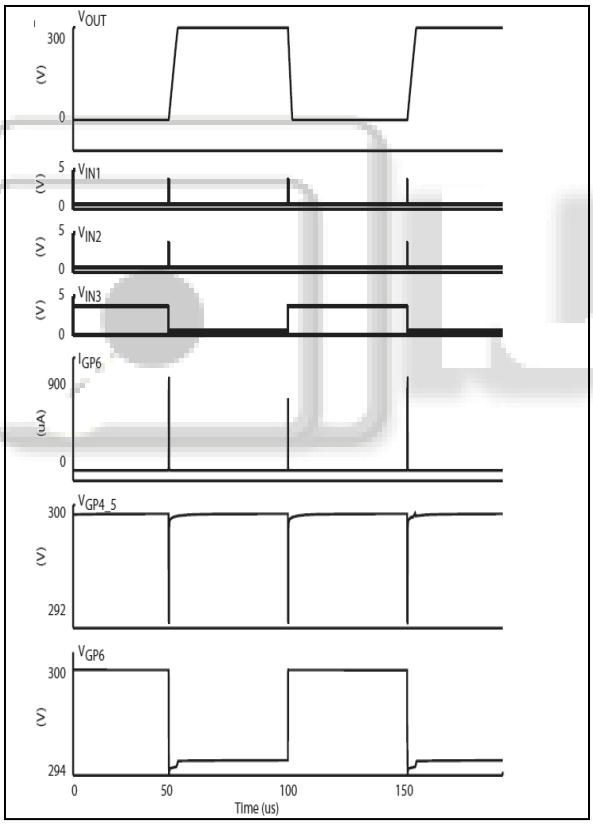

Fig. 4 Simulation results of circuit 4 [5]

The circuit 3 and 4 results are summarized in Table 1. This table shows different parameter consideration.

Parameter	Circuit 3		Circuit 4	Units
	Simulation	Measured	Simulation	
Rise Time	13	14.8	10.25	µs
Fall Time	4.72	6.95	4.74	µs
Slew Rate (Rising)	18.4	15.59	23.6	V/µs
Slew Rate (Falling)	50.7	35.4	53.3	V/µs
TPROP (L-H)	8.08	8.97	6.2	µs
TPROP (H-L)	2.91	4.06	3	µs
Source Current	-179.4	-150.3	-177.8	µA
Sink Current	401.7	311.5	401.7	µA

Table. 1: Summary of circuit 3 & 4

VI. CONCLUSION

The four voltage level shifters are outlined in this survey. First two voltage level shifters are conventional level shifters concentrating to avoid Vds and Vgs breakdown with maintaining full output voltage swing. It was demonstrated in a pseudo-NMOS level-shifter that by means of a current-limiting configuration, the power consumption could be reduced significantly at expense of switching speeds. The improved dynamic level-shifter offers an excellent compromise between performance, area and power at the cost of additional control logic.

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