A 2.5 Ghz LNA Design Using 0.13µm Technology

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Abstract--- Low Noise Amplifier is a"Radio Frequency Amplifier" which amplifies weak signal without introducing internal noise. It is located very close to the "Antenna" to reduce losses in the feed line. It determines the noise performance of the overall system. LNA would offer a large dynamic range that accommodates large signals without distortions and provide good matching to its input and output. In this paper, the design of a Single-Ended LNA operating at 2.5GHz using 0.13µm technology is explained. The tools used for design the single-ended design are Cadence Orcad-Pspice for model verification, Advanced Design System (ADS 2009) for simulation at front-end and Micro-Wind for back-end core layout design.

Keywords: Low Noise Amplifier, 2.5GHz Radio-Frequency, Design of LNA, Analysis of LNA,

I. INTRODUCTION

THE function of low noise amplifier (LNA) is to amplify low level signals to maintain a very low noise. Additionally, for large signal levels, the low noise amplifier will amplify the received signal without introducing any noise, hence eliminate channel interference. Low Noise Amplifier (LNA) plays a crucial role in the receiver designs. LNA is located at the first stage of RF receiver and it has dominant effect on the noise performance of the overall system. It amplifies extremely low signals without adding noise, thus the Signal-to-Noise Ratio (SNR) of the system is preserved. In LNA design, it is necessary to compromise its simultaneous requirements for high gain, low noise figure, stability, good input and output matching.

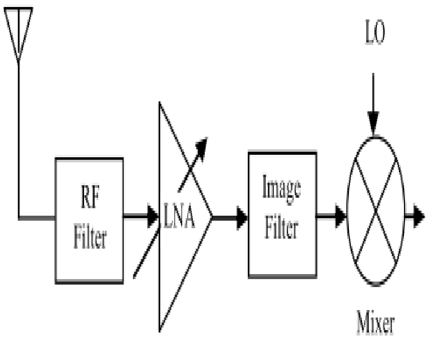

Fig. 1: Basic RF Front-End Receiver Topology

II. SPECIFICATION OF LNA

Si no	Parameter	Specification	Units
1	Frequency	1.9-6	Ghz
2	Noise Figure	<2	dB
3	Gain	<=21	db
4	Power	<40	mW
5	Source &Load Impedance	50	Ω

The main important feature while design an RF-circuit is to first note down the key parameter from any references. There are certain parameters which are very much useful in designing Single-Ended LNA that are being listed with specification on the below given tabular column.

III. DESIGN OF LNA

A. Low Noise Amplifier Topology

Out of the several topologies for narrow band single ended LNA design, an appropriate topology had been selected for low power and low voltage optimized LNA design. Resistor termination common source topology adds noise to the LNA because of the resistor thermal noise. Inductive degeneration common source topology satisfies the specification in very low power consumption, but the isolation is not good enough compared to the cascade inductor source degeneration topology, which can get the similar low noise amplifier performance in very low power consumption. Above all, the cascade inductor source degeneration topology is selected for this design.

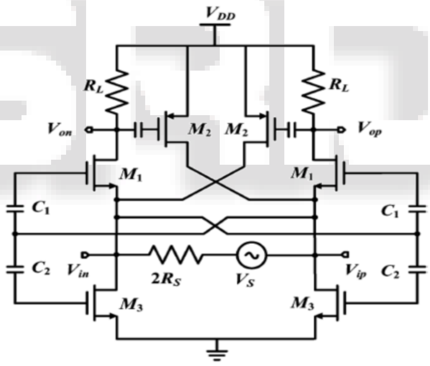

Fig. 2: Schematic of the proposed CGLNA

B. Design of Single-Ended Low Noise Amplifier

positive feedback gain, which varies from 0 to 1 for stability. In this way gm1, can be chosen arbitrarily to values higher than 10 mS without restricting the input matching condition. For example, If $Apos$ is designed to be 0.5 and $Aneg = 1$, then mS for the 50- input matching to be satisfied. Thus, the gain increases. The fully differential positive-negative CGLNA in [17] is shown in Fig. 1(e). Since the positive feedback a way that the impedance matching does not fix the bias current, the current will be a design variable to improve the noise performance. Considering the thermal channel noise, under input matching condition, the noise factor is given by

1) Input Impedance

The two current (shunt) positive feedback paths have the effect of increasing the CGLNA input impedance. Referring to Fig. 2, the input impedance is given by

$$Rin = 1/(gm1(1 + Aneg)(1 - Apos - Bpos)) = 2/(2gm1(1 - Apos - Bpos))$$

Where $Apos = gm2RL$ $Bpos = m3/2gm2$ $and\ Aneg = 1$ Thus, the input matching condition is given by

$$2gm1Rs(1 - Apos - Bpos)$$

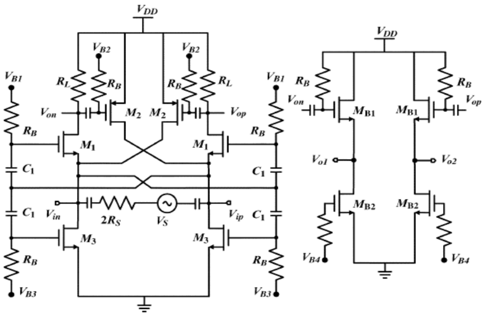

Fig. 3: Schematic of the entire LNA with the output buffer.

2) Stability

The condition of stability is based on the approach of the return ratio (RR) [15]. This approach is used to study the amplifier stability in the presence of multiple feedback loops and to model bidirectional paths between input and output. For the proposed CGLNA

IV. SIMULATION AND LAYOUT RESULTS

A. AC Characteristic Analysis

The main purpose of the simulation is to make the design to be perfect for expected results previously we have designed the circuit for 2.5GHz so to find the expected AC analysis and the output was displayed as such in the below given Fig 4. There are two waveforms which describe the two-different stages of amplification.

The maximum power consumed by the LNA design is about 40mW. The small amplified output shows the first stage of amplification and the higher waveform shows the second stage of amplification, which are shown in the simulation results of AC-Characteristic analysis [Fig-4].

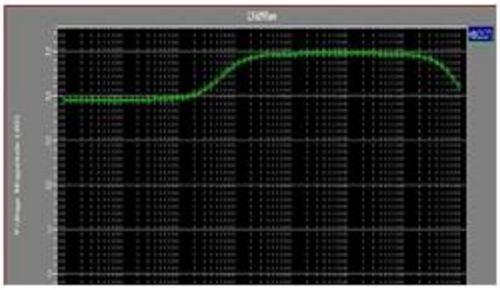

Fig. 4: AC Sweep with 2.5GHz as Output

B. Harmonic Balance Two-Tone Analysis

The stability and frequency spectrum can be analysed by ADS software using harmonic balance and two tone HB test. During this test the circuit is examine whether spurious harmonics generation or not and stability at the carry over range for communication system all standard communication devices undergo this HB-Two Tone Analysis. Hence for this design the expected output is given in Figure 5. This analysis also involves third order intercept (TOI) to the output and input of Single-Ended LNA circuit shown in Figure 3 above. The main and key part of this design is to match the input and output port with general 50 ohm impedances and the complete circuits is designed in cadence Orcad-Pspice for technology model file verification and then it is being simulated

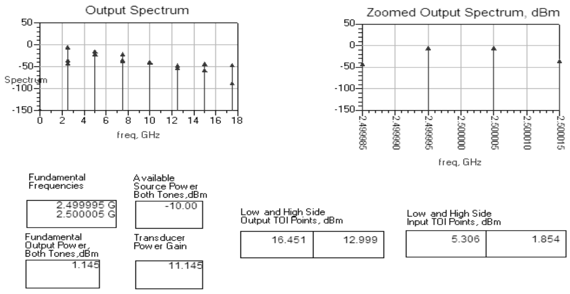

Fig. 5: Harmonic Balance Two-Tone Analysis at 2.5GHz

C. Noise Figure Analysis

Fig. 4 shows a simplified model for the noise sources of the proposed CGLNA. The circuit noise performance is analyzed and its NF is computed assuming that the dominant noise sources are due to the thermal noise of the transistors and load The coupling capacitors,C1 and C2, in Fig. 2 are replaced with short circuits since they are much larger than the gate capacitance of the input transistorsM1 andM3 ,respectively. In this case, the noise due to the source resistance vs the thermal noise due toM2 ,Vn2 , and that due to M3 ,Vn2 , as shown in Fig. 2, create two equal and opposite noise

2	Noise Figure	3	0.55-1.535	dB
3	Gain	15	21	dB
4	Power consumption	30	40	Mw
5	Soure & Load Impedane	50	50	Ω

V. CONCLUSION

An inductorless broadband CGLNA employing noise reduction has been proposed in this paper. The LNA relies on multiple feedbacks to fully decouple the tradeoff between noise and input power matching. The theory shows that the proposed approach reduces the lower limit of the noise performance of the previously reported CGLNAs, allowing for an NF around 1.6 dB. Measurements of a fabricated prototype in 0.13µm CMOS technology show a voltage gain of 21 dB with a 3-dB bandwidth of 1.77 GHz. A minimum NF of 1.65 dB and an of -2.85 dBm are also measured. The measured NF is lower than the best reported NF of CGLNAs. The LNA consumes40mW from a 4.7-V supply

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