A Novel Approach to 3-Bit Flash ADC

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Abstract--- In this paper we have implemented a high speed flash ADC with low power by using threshold inverter quantization technique. The main benefit of the TIQ based CMOS flash ADC design is a simpler comparator design. The proposal is to use digital inverters as analog voltage comparators. This eliminates the requirement of high-gain differential input voltage comparators that are inherently more compound and slower than the digital inverters. The TIQ flash ADC also eliminates the need of reference voltages, which require a resistor ladder circuit. This simplicity in the comparator part provides both high speed and lower power consumption at the same time.

Keywords: ADC architecture, TIQ flash ADC, TC to BC converter, TIQ comparator.

I. Implementation Of The Paper

The technique we are using in our implementation is threshold inverter quantization; high speed CMOS architecture with low power is used. We are using this technique as it is a simpler comparator design in ADC architecture .In the proposed work the idea is to use digital inverters as analog voltage comparators that are essentially more complex and slower than the digital inverters. This idea of using digital inverter eliminates the need of high gain differential input voltage comparator. This technique (TIQ) also eliminates the requirement of the reference voltages which is consists of a resistor ladder circuit. The simplicity present in the circuit of comparator part provides both speed and low power consumption at the same time.

The switching threshold voltage of the quantization inverter is the analog quantization level of digital comparator. It is a reference voltage and is self-determined by the size ratio of NMOS and PMOS. The internal reference voltage, V_m, is defined as the input voltage V_{in} of the quantization inverter when the output voltage equals to input voltage, where both PMOS and NMOS transistors are in saturation. The voltage Vdd is the supply voltage of the process. By changing the widths of the PMOS and NMOS devices with a fixed transistor length, we get different threshold voltages. The value of Vm is expressed in equation below.

$$V_m = \frac{\sqrt{\frac{\mu_p W_p}{\mu_n W_n}}}{1+\sqrt{\frac{\mu_p W_p}{\mu_n W_n}}}\left(V_{dd} - V_{Tp}\right) + V_{Tn}$$

II. TIQ Comparator

It has been acknowledged earlier that a TIQ comparator generates reference voltage internally; the length and width of PMOS and NMOS are varied in order to get desired switching voltage. Here the comparator switching voltage is dependent on the threshold voltage of PMOS and NMOS. To reduce the power consumption of the design, the threshold voltage should not be deviated too much. In contrast, even if the transistor length is kept very small to achieve a high speed, it will have an effect on the output because of the channel noise and results in a nonlinear switching pattern. Therefore the value of the length of the transistor is kept constant at a nominal value and width of transistor is used for generating different switching voltages. In this design low leakage current MOS devices are used in order to keep the power consumption as small as possible, keep Wp / Wn< 1 to reduced power consumption and also to reduced parasitic capacitance.

Comparator No.	L_p, L_n(µm)	W_p(µm)	W_n(µm)	Switching Voltage
1	0.22	0.025	1.6	0.25
2	0.22	0.09	1.6	0.35
3	0.22	0.29	1.6	0.45
4	0.16	0.18	0.42	0.55
5	0.16	0.18	0.12	0.65
6	0.16	0.18	0.03	0.75
7	0.16	0.18	0.015	0.85

Table. 1: Switching voltages of the comparators

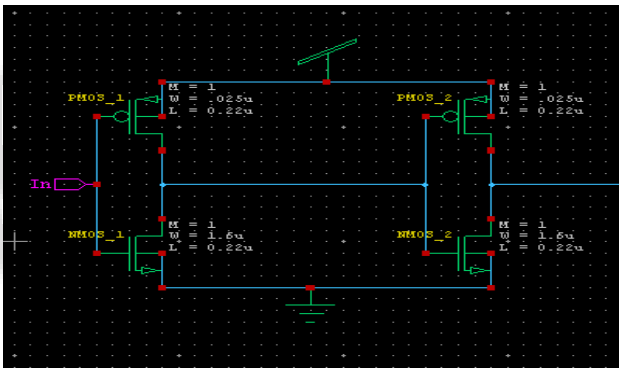

Fig. 1: Schematic of TIQ comparator

In the proposed design the size of the NMOS and PMOS with their minimum and maximum switching voltages are shown in table below. The table below is showing the variation of Wp and Wn on the switching voltage. Wp is first varied for a constant Wn to get its effect on switching voltage and then Wn is varied for a constant Wp. The variation of switching voltage in the table .

III. 3-Bit Flash ADC

The figure below shows the schematic of 3 bit flash ADC which consists of 7 TIQ comparators and a unit of gain booster and a code converter. Code converter which converts the code obtains from gain boos

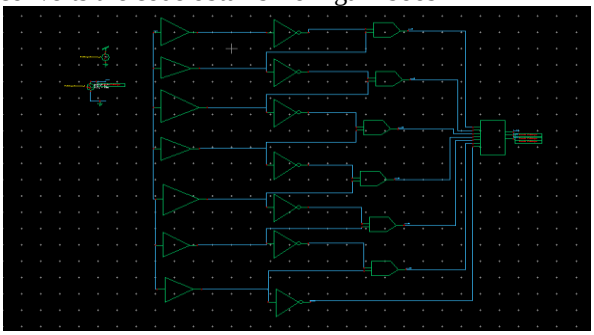

Fig. 2: Schematic Of 3-Bit Flash ADC:

The figure below shows the final output waveform of proposed 3 bit TIQ based ADC on tanner tool.

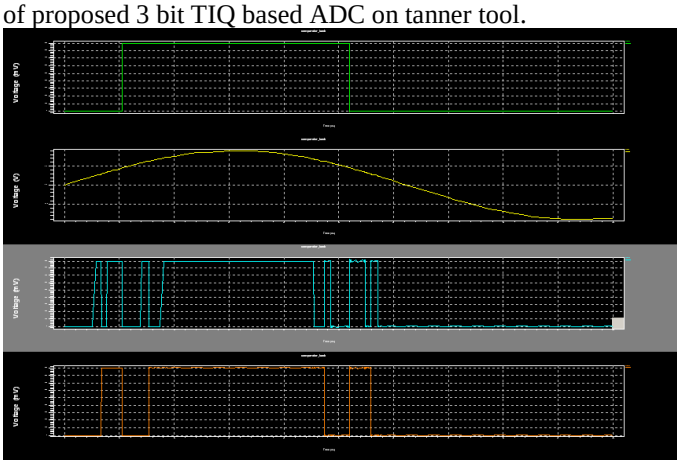

Fig. 3: Final output waveforms of 3-bit flash ADC

IV. Results And Analysis

The 3 bit flash ADC is implemented on 90nm process technology in standard CMOS digital design. And the simulations are done by using Tanner EDA tool. The supply is given 0.9V. The presimulation is done in T-Spice. The leakage power consumption of our implemented flash ADC is also low at 0.9V power supply.

Technology	90nm
Power Supply	0.9V
Resolution	3-bit
Frequency	100KHz
Leakage Power	18nW
Average Power Consumed	870µW

Table. 2: Specifications of Flash ADC

Leakage Current	Power Supply	Leakage Power
20 nA	0.9V	18nW
100nA	0.9V	140nW

Table. 3: Summary of leakage power of flash ADC

V. Conclusion & Future Work

An uncomplicated and fast flash ADC has been implemented which consists of two cascaded inverters as comparators, called as threshold inverter quantization (TIQ) technique. The TIQ flash ADC provides higher data sampling rate and operates at low voltage and also low power consumption. It is highly suitable for the complete SoC integration using the standard CMOS digital process. As a future work we will improve the design in many ways. For low power design it is required to generate the MOSFET width automatically so that the power consumption of TIQ comparator block can be more reduced. Moreover the time interleaved conception can be used to increase speed.

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