Design and Analysis of a Full Adder Circuit using XOR and AND Gates Pass Transistors and Transmission Gates

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Abstract---This paper presents a complex full adder design having higher computing speed, lower operating voltage and low power consumption as these all are requirements of a VLSI design system. The proposed full adder design makes use of low power designs such as XOR and AND gates pass transistors and transmission gates. The simulation results are matched with the conventional cell by standard implementation. In this circuit design power consumption is done upto 40% by an addition. As the word length of the adder decreases the power consumption decreases significantly. We describe that how efficiently XOR and AND gates are realized to a general full adder circuit based on a pass transistor logic. The simulation results are compared with the standard simulation of the tool proposed in the project.

Keywords: Full adder, Low operating power, High computing speed, pass transistors.

I. INTRODUCTION

Various arithmetic operations are used in VLSI technology such as addition, subtraction, multiplication and accumulation operations. The basic building block of the VLSI design circuits and enhancement of the VLSI modules is a one bit full adder circuit. The future VLSI systems propose to be compared on the basis of speed, power consumption and area utilization. In this paper a one bit full adder is presented which consumes less power than a standard full adder cell.

A. *Power Consumption Modules in A Cmos:* Basically there are three main power consuming components or stages in a CMOS circuit i.e.

- Switching Power- It consumes the power a circuit in charging and discharging of the
- Capacitances during switching of the transistors.
- Short circuit power- Consumes the power in short circuiting the leakage current flowing from power supply to ground during transistor switching.
- Static power- It consumes the power due to leakage current flowing through the circuit while the circuit is in stable state

The switching power and short circuit power consumptions are referred to as dynamic power consumptions while in the third state the power is consumed dynamically but the state of the circuit changes.

The total power is given by the equation

$$P_{total} = V_{dd} f_{clk} \sum i v_{swing} c_{load} p_i + V_{dd} \sum i I_{isc} + V_{dd} I_i$$

$$P_{total} = V_{dd} f_{clk} \sum i v_{swing} c_{load} p_i + V_{dd} \sum i I_{isc} + V_{dd}$$

Where V_{dd} is the power supply voltage, V_{swing} voltage swing of the output which is equal to V_{dd}, C_{load} load capacitance at node, F_{clks} system clock frequency, Pi switching activity at node I, I_{isc} short circuit at node, L_i leakage current.

B. *1-Bit Full Adder Cells:* The one bit full adder functionality can be demonstrated by the following equation:

$$Sum = (A\ XOR\ B)\ XOR\ C_{in}$$

$$C_{out} = A.B + C_{in}(A\ XOR\ B)$$

given three one bit inputs as A, B and C_{in} and desired to generate the two one bit outputs i.e sum and output.

C. *Three 1-Bit Adder Cells:* 10T cell- It contains pmos and nmos and three V_{pulse} is added in it and one V_{dc} is connected to the port of the inverter and we take 1.8 voltage supply and rise time , fall time and width can be taken in diferent ratio in V_{pulse}.

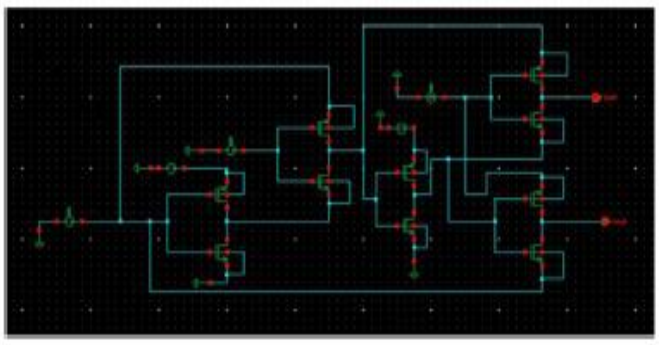

Fig. 1: T cell

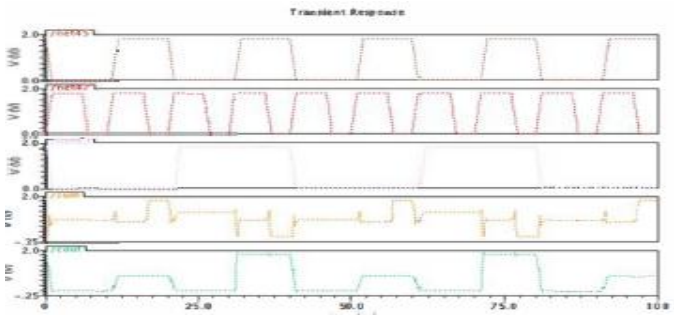

Fig. 2: Output Waveform Of 10T

The proposed adder circuit diagram is constructed by combining all the designed components as shown in Figure. When the inputs A=B=O, the XOR gate will introduce 1- VT loss and this loss causes the nMOS transistor(Nl) of the inverter not to be completely turned off(weak inversion) and results in subthreshold leakage current. The subthreshold leakage current causes higher power dissipation in the circuit. To avoid this leakage

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current problem, we have introduced a mos (Pstack) transistor in series with the pull up transistor of the inverter as shown in Figure 2. This extra transistor gives lower leakage as well as ensures that pull up pMOS is completely off when either inputs (A or B) are high. The added transistor will increase the overall area on chip and slightly degrades the response of carry-out because pMOS is slower device.

D. *Proposed Future Work:*

11T Cell: It is used for better efficiency and higher computation speed than the previous cell discussed. We propose to make a cell which contains nMOS and pMOS and three Vpulse is added in it and rest of the functioning is done just same as that of 10T cell.

1) *16T Cell:* It also contains complementary mos and similar to that of 10T and 11T the ratios of rise time, fall time and width can be varied according to $V_{pulse.}$

Accordingly we will generate schematic of the 11T cell and 16T and compare with the 10T cell and also we will compare the power consumption and size of the area used.

II. Conclusion

An approach to a low power 1-bit full adder has been done to optimize the power consumption and data computing process in VLSI design and a high performance and high speed is being taken into consideration for the proposed research work. The schematics of 10T, 11T and 16T will be demonstrated as research work and the leakage power will be calculated at the end. The main work is to lower the operating voltage and minimize the area and reduce the leakage current.

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