Design Of An Optimized Full Adder And Ripple Carry Adder Using Reversible Logic.

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Abstract—the full adder is the basic block building that widely used in digital circuits such as the ALU and multiplier. One of the most promising technologies in designing low power circuits is reversible logic or computing. In the VLSI design of today's circuits suffered from power consumption which leads to power dissipation in the circuits. To reduce the power dissipation in circuits, reversible logic is used. There are different types of logic gates are used to minimize the power dissipation and chip area such as NOT gate, Controlled NOT gate, Controlled Controlled NOT gate and Fredkin gate. In this research work some basic circuitry such as full adder and ripple carry adder with 45nm technology are highlighted.The proposed design is compare CMOS full adder and 4 bit Ripple carry adder with time delay and power dissipation. Power consumption is reduced 70% compared to conventional full adder and the time delay of the circuit is 19.88 nsec and 19.78 nsec for sum and carry respectively.

Keywords:- Reversible logic, Fredkin gate, 4 Bit BCD adder power consumption and CMOS full adder.

I. Introduction

Every day new technology which is faster, smaller and more complex than its predecessor is being developed. To achieve greater speed, increase clock frequency and increase in number of transistors mounted onto a chip to achieve complexity of a conventional system results in increased power consumption. All the millions of gates and transistor perform some operation which leads to heat dissipation in the circuit is called irreversibility[1]. While performing the logical operation some information has been erased or lost and some amount heat dissipated[3]. As per Landauer scientist said that, for irreversible logic, each bit of information lost generates kTln2 Joules of heat energy, where k is Boltzmann's constant and T is absolute temperature while performed the operation. Reversible logic operations do not lose the information and does not dissipate any heat[7]. Reversible logic reduces the heat dissipation and allowing the higher densities as well as higher speed[1]. It plays very vital role in the field of digital circuits and nanotechnology computing. In reversible logic, there is one to one mapping between input vectors and output vectors[5]. For instance, three inputs are there and equal number of output also there. Any deterministic device to be reversible is that its input and output be uniquely retrievable from each other and vice versa then it is called logically reversible.

In this paper, all circuits are implemented by NMOS pass transistor only. All internal gates of the adder, ripple carry adder and BCD adder are designed by using controlled not gate, controlled controlled not gate and Feyman gate. In reversible logic, garbage input and garbage output concept is also used (GIGO). Garbage input and Garbage output means that input and output are not used for further processing in cascading to digital circuits. By comparing this technique to a CMOS technique number of transistors has been reduced and offers an advantage of low power consumption, high switching speed, lower area and lower parasitic capacitance[3]. Reversible logic circuits have promising features are as follows:

- Use the less number of reversible gates.
- Use the less number of garbage outputs.
- Use the less number of constant inputs.

II. Review Of Reversible Gates

Reversible gates that have one-to-one mapping between vectors of inputs and outputs; thus the vector of input states can be always reconstructed from the vector of output states. For instance, N X N reversible logic gates means N number of input and same number of output. Reversible gates comprises Feyman gate, Fredkin gate and Toffoli gate.

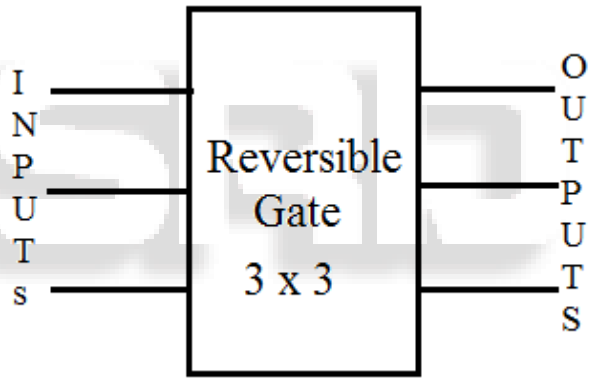

Fig. 1: Generalize Diagram Of Reversible Gate.

A. Controlled Not

Several basic gates are present in reversible logic such as controlled NOT gate, controlled controlled gate and Feynman gate. In Controlled NOT gate, logic performed by (A,B) are the input vectors and (P,Q) are the output vectors as shown in fig 1. This operation performed for only two input logic gates. The first one is control inputs (A, Abar) they control the ON and OFF states of the transistors and thus transfer data from input to output by the use of input terminal (B, Bbar) For instance, input terminal A=1, B=1 and corresponding inverted inputs are Abar =0, Bbar=0.The input A controls the transistors T1 and T3 and Abar controls the transistors T2 and T4. If, A=1 and B=1 then T1 and T3 are in ON states and T2 and T4 are in OFF states and we get the pass signal (B, B^) in the corresponding output lines P=1, P =0 and Q=0, Q =1. Now by the reverse logic, P and Pbar are the input and pass signals will be a Q and Qbar and the outputs will be A. Abar and B, Bbar. The speciality of this circuit, we can use forward operation as well as reverse mode operation.

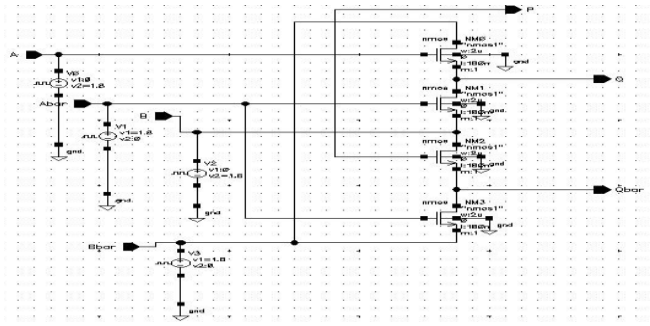

Fig. 2: Controlled Not Gate

TABLE I. Truth Table Controlled NOT

A	B	P	Q
0	0	0	0
0	1	0	1
1	0	1	1
1	1	1	0

The CONTROLLED NOT can be realized
When P = A and
If A = 0, then Q = B;
Else Q = NOTB So we can write Q = A XOR B

B. Controlled Controlled Not

The Controlled Controlled Not reversible gate is quite similar to Controlled NOT gate, except that controlling of transistors in Controlled Controlled NOT gate occurs twice while propagating the signal from input to output.

The Controlled Controlled NOT can be realized

When P = A, Q = B and If A AND B = 0; Then R= C ,

Else R = NOT C So R = [A AND B] XOR C.

TABLE II. Truth Table Controlled Controlled Not

A	B	C	P	Q	R
0	0	0	0	0	0
0	0	1	0	0	1
0	1	0	0	1	0
0	1	1	0	1	1
1	0	0	1	0	0
1	0	1	1	0	1
1	1	0	1	1	1
1	1	1	1	1	0

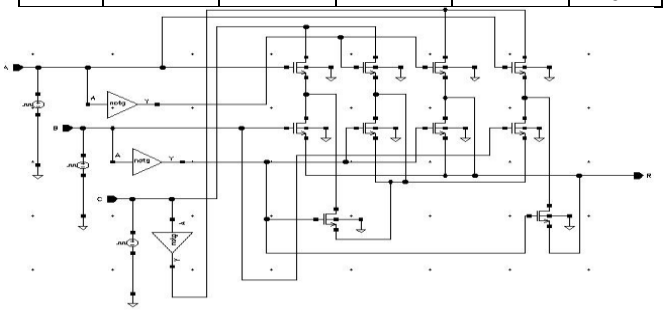

Fig. 3: Circuit Diagram for Controlled Controlled Not Gate

III. Design Of Reversible Full Adder

In CMOS Full Adders, there are two section first one is input and another is output section. The input section generally contains three inputs A, B and Carry in(Cin).The output section contains two output Sum and Carry Out (C0). For different combination of input values, the conventional Full Adder sometimes generates the same outputs. This circuit does not follow the reversible logic. In reversible, by judging the output we can determine the corresponding input. Thus the Adder can be operated reversibly. To get the uniqueness of the output values necessary to add some extra bits in both inputs as well as output section. As shown in the truth table, P(preset) is added in the input section and Garbage output(G1 and G2) is added in the output section. The truth table for reversible Full Adder has been shown in Table 5. The implementation of Full Adder using reversible logic is as follows:

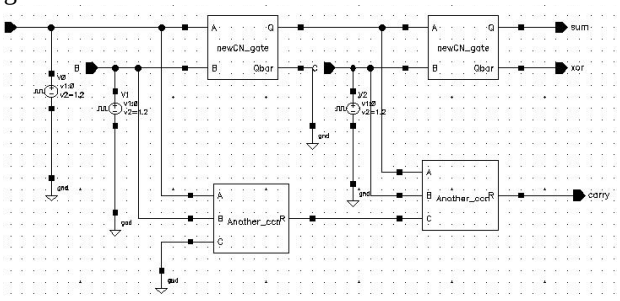

Fig. 4: Reversible Full Adder

TABLE III: Truth table of Reversible Full Adder

A	B	Ci	P	SUM	CARRY	G1	G2
0	0	0	0	0	0	0	0
0	0	0	1	1	0	0	0
0	0	1	0	0	1	0	0
0	0	1	1	1	1	0	0
0	1	0	0	0	1	0	1
0	1	0	1	1	1	0	1
0	1	1	0	1	0	0	1
0	1	1	1	0	0	0	1
1	0	0	0	0	1	1	1
1	0	0	1	1	0	1	1
1	0	1	0	0	0	1	1
1	0	1	1	1	0	1	1
1	1	0	0	1	0	1	0
1	1	0	1	0	0	1	0
1	1	1	0	1	1	1	0
1	1	1	1	0	1	1	0

IV. Design Ripple Carry Adder.

Arithmetic operations like adder, subtraction, multiplication and division are basic operation implemented in digital computing using basic gates such as AND,OR and NAND gate etc. If all operation are implemented by addition it is easy to perform multiplication (repeated addition) and division (repeated multiplication).Half adder add two binary bits and give the result in the form of the sum and carry. Each full adder inputs a Cin, which is the Cout of the previous adder. This kind of adder is a Ripple Carry Adder, since each carry bit "ripples" to the next full adder.

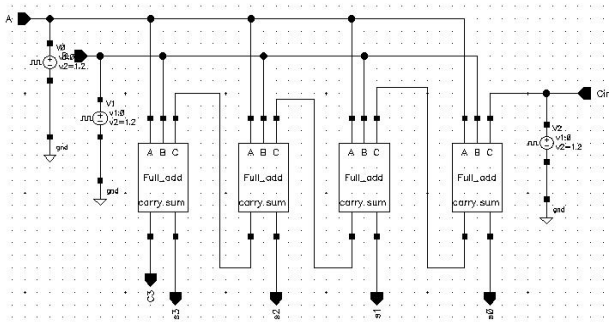

Fig. 5: 4bit Ripple Carry Adder.

V. RESULTS AND DISCUSSION

In this research work used Cadence tool environment version 6.32(Virtuoso) with 45nm techonolgy. As compared with the above technique to existing CMOS Adder is having a reduced number of transistors and low power consumption. Reduced number of transistor circuit may have lower capacitance and high switching speed. The time delay also gets reduced.

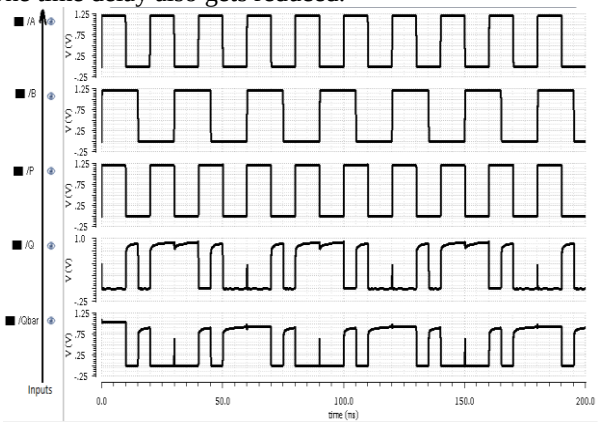

Fig. 6: Controlled Not Gate Waveform.

The CONTROLLED NOT can be realized
When P = A and
If A = 0, then Q = B;
Else Q = NOTB So we can write Q = A XOR B .
If A=1 and B=1,P=A and ouput Q = 0, Qbar = 1
A= 0 and B=1 then Q = 1 and Qbar = 0 that means performed the Exclusive OR operation.

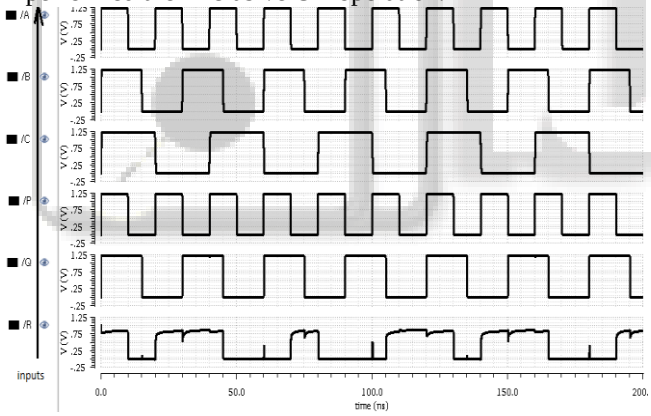

Fig. 7: Waveform of Controlled Controlled Not Gate.

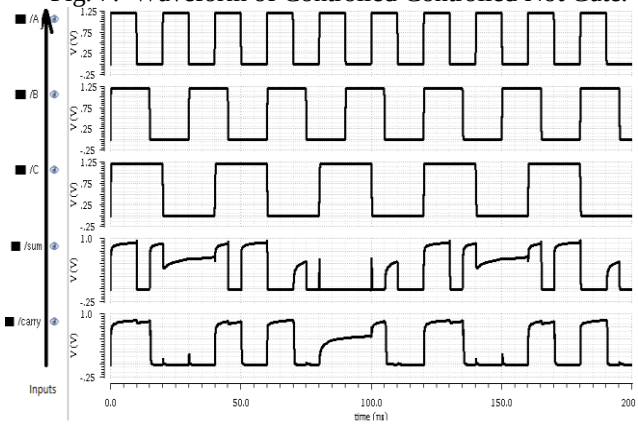

Fig. 8: Reversible Full Adder.

If A=1,B=0,C=0 then sum=1 and carry =0
A=1.B=1,C=0 then sum =0 and carry =1
A=1,B=1,C=1 then sum = 1and carry =1.

Table IV: Power comparison of Full adder circuit

Circuit Name	Power Dissipation(uW)
Full adder using CMOS Logic	3.06
Full adder using Reversible Logic	0.914

The time delay of reversible full adder as follow:

- Sum with respect to input is **19.88 nsec**.
- Carry with respect to input is **19.78 nsec**.

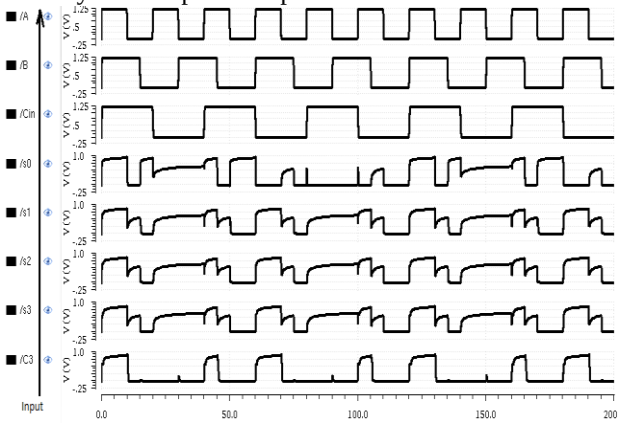

Fig. 9: Waveform Of Ripple Carry Adder.

Table IV: Power Comparison of Ripple Carry Adder.

Circuit Name	Power Dissipation (Uw)
Ripple Carry Adder Using CMOS Logic	12.94
Ripple Carry Adder Using Reversible Logic	3.74

VI. CONCLUSION

The implementation of full adder and ripple carry adder by using a Feynman logic gate .In this paper proposed a novel design for the implementation of reversible full adder and ripple carry adder is compared to existing work. The circuit proves to be 70% power efficient than existing CMOS adder. Simulation of these circuits has been done and proved to be useful for the design of future computing techniques like low power digital circuits, nanotechnology and quantum computers.

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