Design and Implementation of 6-bit Successive Approximation Register (SAR) Analog to Digital Convertor (ADC) using 45 Nano-meter Technology

Nirav A. Mehta[1], Bharat H. Nagpara[2]
[1,2]Electronics & Communication Department
[1, 2] C. U. Shah College of Engineering and Technology (GTU), Wadhwan city, Gujarat

Abstract---In this paper, The Design and Implementation of Successive Approximation Register (SAR) Analog to Digital Convertor (ADC) in 45 nm technology using TANNER TOOL, V15 is presented. The simulation results show the transient analysis waveforms of different blocks of SAR ADC and also the result of 6-bit SAR ADC. The mainly four blocks are in the SAR ADC. The blocks are Sample and Hold, Dynamic Comparator, SAR Logic and DAC Logic. Here the DAC logic is used for the feedback to comparator and its made from the charge scaling capacitor. This design is for low power and low area consumption in chip or circuit design and compared with each other. These SAR ADC is high speed switching and low power consumption with compares to any other ADC.

Keywords: CMOS, Sample and Hold, Comparator, SAR Logic, DAC Logic, TANNER TOOL

I. INTRODUCTION

In an analog to digital system the quality of the digital signal is main criteria, for long distance transmission it is necessary to convert analog signal into digital signal at input side, same as convert digital signal into analog signal at output side. CMOS technologies have been used for low power applications; also submicron processes have allowed CMOS to achieve low power. In this paper different blocks are available which are used in A to D converter using 45nm technology are presented. The block diagram of SAR ADC is shown below:

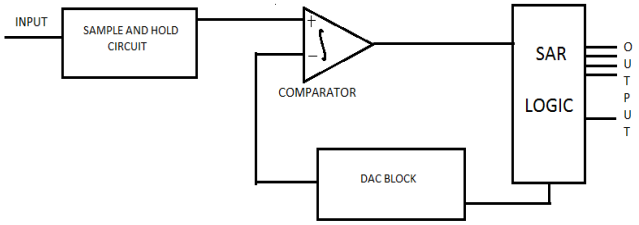

Fig. 1: Block Diagram of SAR ADC

Comparator is the only analog block of a SAR ADC and performs the actual conversion. It compares the analog sampled input to the analog output of the DAC and generates digital output of '0' or '1' which will be used in the SAR logic. Accuracy and speed of the comparator are two important factors. The comparator offset voltage does not affect the overall linearity of the converter because it can be represented as a voltage source in series with Sample & hold output, indicating that offset voltage simply adds to analog input and hence appears as an offset in the overall characteristics. Consequently the comparator can be designed for high speed operation in high resolution systems.

In general, Sample and hold circuit contains a switch and a capacitor. The switch is made from the CMOS with using NMOS and PMOS as Transmission Gate. A sampling switch is the front-end of the ADC and requires careful attention during the design. The implementation of the switch depends on the required bandwidth and accuracy. Noise is out of concern because it is determined by the sampling capacitance. The sampling switch can be designed with a single NMOS or PMOS transistor, a complementary CMOS switch or more complicated bootstrapping circuitry can be used. The simplest implementation is always preferable but rarely feasible. In the tracking mode, when the sampling signal is high and the switch is connected, it tracks the analog input signal. Then, it holds the value when the sampling signal turns to low in the hold mode. In this case, sample and hold provides a constant voltage at the input of the ADC during conversion. Regardless of the type of S/H, sampling operation has a great impact on the dynamic performance of the ADC such as SNDR.

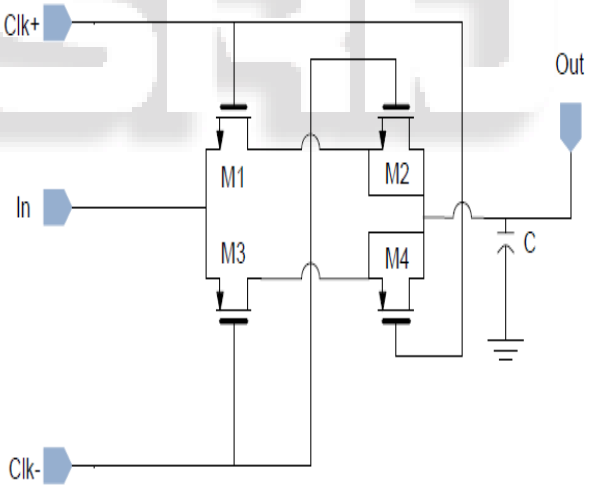

Fig. 2: Sample and Hold Circuit

A CMOS switch is able to cover a rail-to-rail input range, however, due to the low supply voltage there is a voltage range in which both NMOS and PMOS transistors are in the sub-threshold region. As a result, a conductance gap in the middle of the input range appears, degrading the linearity. Obviously, increasing the width of the transistors makes a switch more linear, but as transistors get larger, various dynamic effects start to degrade their linearity. These effects occur due to the charge redistribution processes between the voltage dependent parasitic capacitances of the transistors and a sampling capacitor. Here the value of capacitor is 0.05pF for sampling and hold.

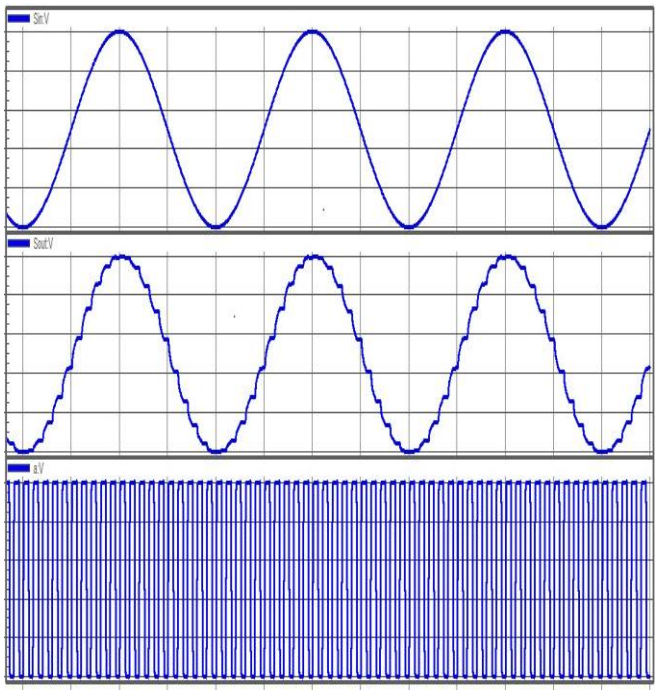

Fig. 3: Result of sample and hold

II. DYNAMIC LATCHED COMPARATOR

Latch only comparators are clocked comparators. They operate based on amplification and positive feedback. An example of a latched only comparator is shown in Figure.

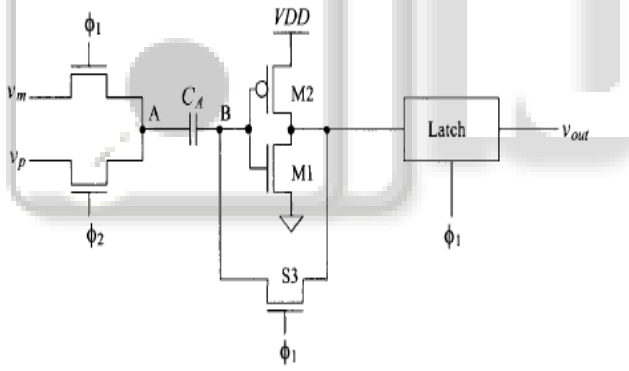

Fig. 4: Dynamic latched comparator circuit

Figure shows the operation of the comparator. There are two operation phases, reset phase and regeneration or evaluation phase. In the reset phase, the output nodes are charged to supply voltage or discharged to the ground depending on the architecture of comparator. During the reset phase, the comparator tracks the input, and then in the regeneration phase the positive feedback produces a digital value at the comparator output. One of the advantages of dynamic latched comparators is their power efficiency since they only consume power in regeneration phase and there is no static power consumption in the reset phase.

Dynamic latched architecture is the most power efficient comparator, however, it introduces large input referred offset which makes it unappealing for high resolution ADCs. This effect can be reduced by increasing the width of input transistors in differential pair. Employing offset cancelation techniques in the comparator implementation is also an effective approach to mitigate this problem. Furthermore, the offset voltage can be reduced by using a pre-amplifier which is previously described as a latched comparator with

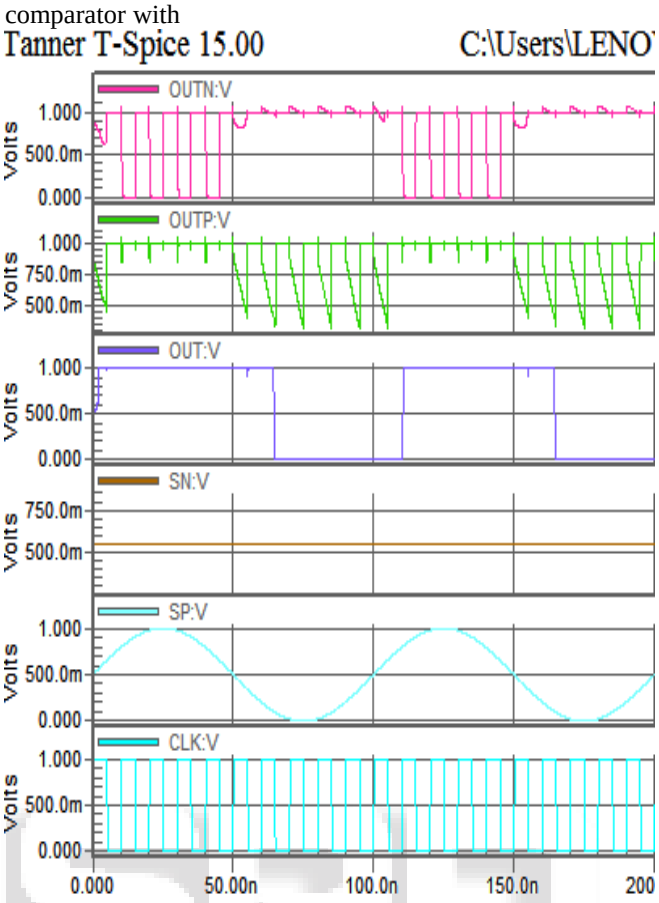

Fig. 5: Dynamic latched comparator circuit result

Pre amplifier. However, in all the mentioned methods, offset reduction is achieved at the cost of more power consumption.

Latched comparators are fast and are suited to be used in high speed ADCs. In order to derive the delay equation, the latched comparator can be modeled as a single pole comparator with positive feedback. The delay time of this comparator is calculated as below:

$$T_d = \frac{C}{g_m} \ln\left(\frac{V_{out}}{V_{in}}\right)$$

III. SAR LOGIC

Successive approximation register ADC implements the binary search algorithm using SAR control logic. In general, there are mainly two fundamentally different approaches to designing the SAR logic. The first one which is proposed by Anderson consists of a ring counter and a shift register. At least 2N flip flops are employed in this kind of SAR . The other, which is proposed by Rossi, contains N flip flops and some combinational logic . SAR control logic determines the value of bits sequentially based on the result of the comparator. Each conversion takes 12 clock cycles. In the first clock cycle, SAR is in the reset mode and all the outputs are zero. In the next ten clock cycles, data is converted and each bit is determined sequentially. The last cycle is for storing the results of the complete conversion.

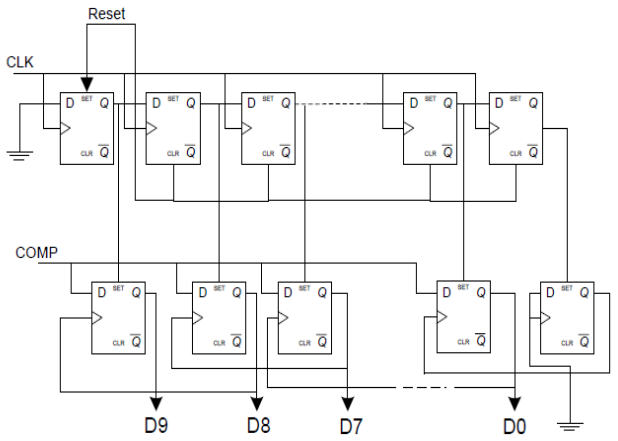

Fig. 6: SAR Logic

In each clock cycle, one of the outputs in the ring counter sets a Flip Flop in the code register. The output of this Flip Flop which is set by the ring counter is used as the clock signal for the previous Flip Flop. At rising edge of the clock, this Flip Flop loads the result from the comparator. Figure shows the transient response. At the end of each conversion, EOC signal turns to high. This type of SAR logic, converts each sample in 12 clock cycles.

The Flip Flops which are employed in this structure are set-reset D-FFs. For low power purpose, transmission gate based Flip Flops are used. Minimum size transistors with double length are chosen for improving the power performance. The schematic of the DFF is illustrated in Figure 4.3. In order to decrease the leakage power even more while simultaneously maintaining the speed, high threshold voltage transistors are used in the noncritical paths and low-VT transistors in the critical path. Thus, this dual threshold approach provides high performance Flip-Flops.

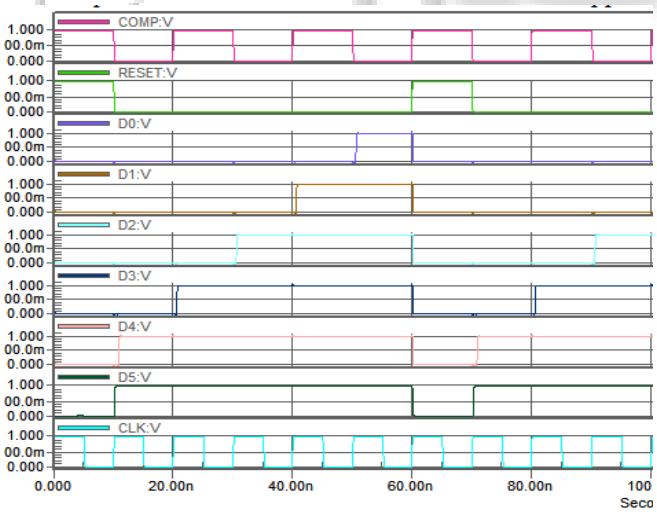

Fig. 7: Result of SAR Logic

IV. DAC LOGIC

The digital to analog converter (DAC) converts the digital word at the output of the SAR logic to an analog value. Then in the comparator, this value is compared to the input signal. In the capacitive DAC with inherent Sample and Hold, the sampling operation is performed by DAC and is called charge redistribution DAC. Nowadays, charge redistribution DACs are commonly used. They consume less power and induce less mismatch errors compared to the resistive based DAC. Charge redistribution DAC has fast conversion time. Moreover, they are fabricated easily . In the following three different architectures of capacitive DAC are presented.

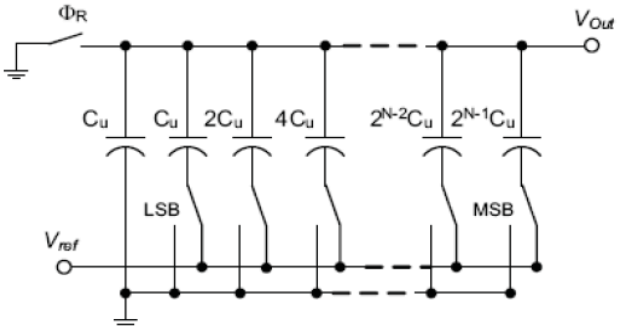

Fig. 8: Binary Weighted Capacitor

An N-bit binary-weighted capacitor array is shown in Figure 3.5. It consists of scaled binary capacitors, i.e., 2N-1C, 2N-2C… 2C, C, C. The last capacitor is a dummy that has equal value as the LSB capacitor. Thus, the total value of the capacitors is 2NC. First, in the reset phase all the bottom plates are grounded. During the redistribution mode in which the actual conversion is performed, based on the provided digital code, the switches are connected to either Vref or ground. The occupied area and power consumption of the BWC is increased with the increase of the resolution.

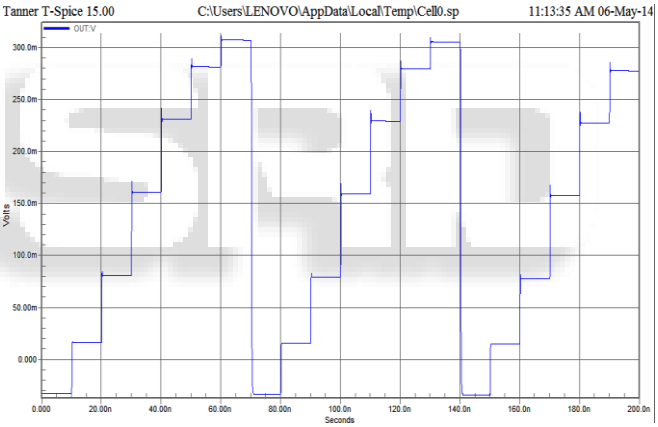

Fig. 9: Result of DAC Logic

V. 6-BIT SAR ADC

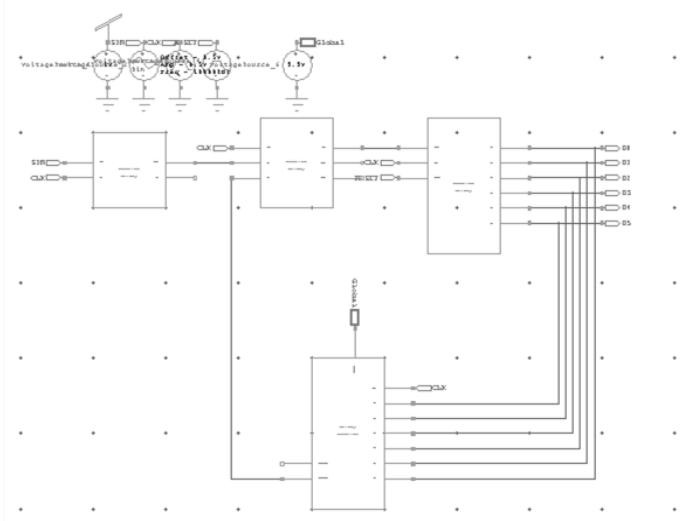

Fig. 10: 6-bit SAR ADC

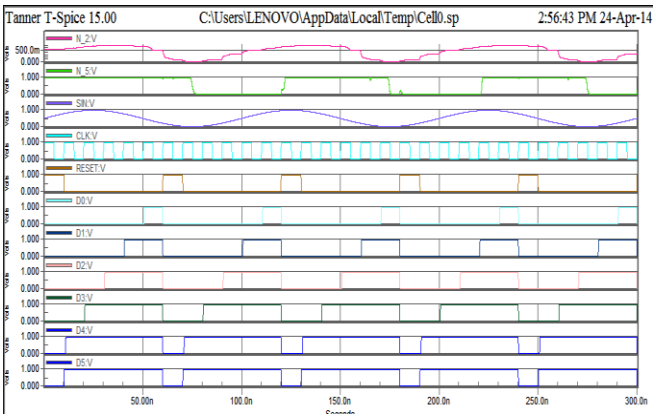

Fig. 11: Result of 6-bit SAR ADC

VI. COMPARISON

By comparing the simulation results of all blocks and also the final result of 6-bit SAR ADC, conclude that the results are very good and with compare to other it is low power consumption and relatively its require small area. Every blocks of ADC gives perfect result and there is no any distortion is occur in result of outputs. So that the output result of SAR ADC in 45-nm is good with compare to any other 90,65,or 180-nm.

REFERENCES

[1] Bob Verbruggen, Masao Iriguchi, Manuel de la Guia Solaz, Guy Glorieux, Kazuaki Deguchi, Badr Malki, Jan Craninckx. "A 2.1mW 11b 410MS/s Dynamic Pipelined SAR ADC with Background Calibration in 28nm Digital CMOS." IEEE Simposium On VLSI Circuits Digest Of Technical Papers 2013.

[2] Tuan-Vu Cao, Snorre Aunet, Trond Ytterdal. "A 9-bit 50MS/s Asynchronous SAR ADC in 28nm CMOS." IEEE 2012.

[3] Ron Kapusta, Senior Member, IEEE, Junhua Shen, Member, IEEE, Steven Decker, Member, IEEE, Hongxing Li, Eitake Ibaragi, and Haiyang Zhu. "A 14b 80MS/s SAR ADC with 73.6dB SNDR in 65nm CMOS." IEEE Journel Of Solid State Circuits, VOL-28, NO-12, December-2013

[4] Chao Yuan and Yvonne Y. H. Lam. "A 281-nW 43.3 fJ/conversion step 8-enob 25-kS/s asynchronous SAR ADC in 65nm CMOS for biomedical applications." IEEE 2013.

[5] Wen-Lan Wu, Yan Zhu, Li Ding, Chi-Hang Chan, U-Fat Chio, Sai-Weng Sin, Seng-Pan U, Rui Paulo Martins. "A 0.6V 8b 100MS/s SAR ADC with minimized DAC capacitance and switching energy in 65nm CMOS." IEEE 2013.

[6] Jun Ma, Yawei Guo, Li Li, Yue Wu, Xu Cheng, Xiaoyang Zeng. "A low power 10-bit 100MS/s SAR ADC in 65nm CMOS." IEEE 2011

[7] Ehsan Zhian Tabasy, Ayman Shafik, Keytaek Lee, Sebastian Hoyos, Samuel Palermo. "A 6b 10GS/s Tf SAR ADC with Embedded 2-tap FFE/1-tap DFE in 65nm CMOS." 2013 Symposium on VLSI Circuits Digest of Technical Papers.

[8] Zule Xu, Masaya Miyahara, and Akira Matsuzawa. "Alps Resolution Integrator Based Time to Digital Convertor using a SAR ADC in 90nm CMOS." IEEE 2013

[9] Chang-Yuan Liou, Chih-Cheng Hsieh. "A 2.4 to 5.2 Fj/conversion step 10b 0.5 to 4MS/s SAR ADC with charge Average Switching DAC in 90nm CMOS." IEEE International Solid-State Circuits Conference 2013.

[10] Geert Van der Plas, Member, IEEE, and Bob Verbruggen, Student Member, IEEE. "A 150MS/s 133µm 7bit ADC in 90nm Digital CMOS." . IEEE JOURNAL OF SOLID-STATE CIRCUITS, VOL. 43, NO. 12, DECEMBER 2008.

[11] R. Jcob Baker. "CMOS citcuit design, layout and simulation." Second Edition 2002, ISBN-987-81-265-2037-4.

[12] Sung-Mo kang, Yusuf Leblebici. "CMOS digital integraed circuit analysis and design." 3rd Edition

